17.4 A Batteryless 19µW MICS/ISM-Band Energy Harvesting Body Area Sensor Node SoC

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Recent advances in ultra-low power chip design techniques, many originally targeting wireless sensor networks, will enable a new generation of body-worn devices for health monitoring. We utilize the state-of-the-art in low power RF transmitters, low voltage boost circuits, subthreshold processing, biosignal front-ends, dynamic power management, and energy harvesting to realize an integrated reconfigurable wireless body-area-sensor node (BASN) SoC capable of autonomous power management for battery-free operation.

Conventional wireless sensors are powered from a battery (Fig. 17.4.1), limiting node lifetime. In contrast, we propose a wireless BASN chip powered by energy harvested from human body heat using a thermoelectric generator (TEG). This, in conjunction with a programmable power management system, allows for indefinite operation of the chip while worn.

Figure 17.4.2 illustrates the system block diagram comprising four sections. An analog front-end (AFE) with programmable gain and a successive-approximation (SAR) ADC amplifies and digitizes signals as low as a few µVs. An energy harvesting/supply regulation section boosts a voltage source as low as 30mV up to a regulated 1.35V supply. A subthreshold digital section performs data processing, mode control, and power management. The energy on the storage capacitor informs power and clock gating. This, coupled with a programmable SC regulator, enables dynamic voltage scaling (DVS). The digital section includes a custom digital power management (DPM) processor, general purpose microprocessor (MCU), programmable FIR, 1.5kB instruction SRAM / ROM, 4kB data SRAM, and dedicated accelerators for ECG heart rate (R-R) extraction, atrial fibrillation (AFib) detection, and EMG band energy calculation. Finally, a sub-mW 400/433MHz MICS/ISM band transmitter performs BFSK transmission up to 200kbps.

The chip has four independently selectable ESD-protected biosignal input channels, consisting of fully-differential chopper-stabilized low-noise amplifiers (LNA) and variable-gain amplifiers (VGA). Our amplifiers provide digitally-programmable gain (40-78dB) from DC to 320Hz at 3µW/channel. A 5-input mux allows the on-chip sub-µW 8-bit SAR ADC to sample any of the four channels as well as the V_{BOOST} node for monitoring stored energy. The digitized V_{BOOST} value is sent to the DPM block, while the digitized biosignal data is sent to the digital accelerators.

A hybrid energy harvesting subsystem allows operation from RF and/or thermoelectric power sources. Small body-worn TEGs typically provide very low output voltages (<100mV), so we employ an ultra-low voltage boost converter capable of boosting voltages as low as 30mV [1]. To initialize the control circuitry of the boost converter, the V_{BOOST} node must be charged to 600mV. This one-time kick-start (Fig. 17.4.1) is provided wirelessly through an RF rectifier front-end with incident power as low as -10dBm. The node will then continue to run indefinitely from the TEG. Figure 17.4.3 details the energy harvesting/supply regulation section. On-chip supply regulation is provided by four sub-µW linear regulators: 1.2V (AFE), 0.5V (DSP), 1.0V (TX LO), 0.5V (TX PA). A programmable switched-cap DC-DC converter provides an output from 0.25V to 1V in 50mV steps. A power-on-reset (POR) is integrated, and an on-chip clamp limits V_{BOOST} to 1.4V to provide over-voltage protection from RF signals. The DPM is an always-on custom Instruction Set Architecture (ISA) MCU that implements a closed-loop power management scheme, controls power- and clock-gating, voltage regulation, time delays, sampling rate, memory access, and data flow on the chip. To manage power and prevent node death, the DPM monitors the digitized V_{BOOST} and changes the node operating mode in a "stoplight" fashion at programmable threshold values. Normal operation is "green" mode (e.g., V_{BOOST} > 1.3V) where all blocks are active. In "yellow" (1.1V < V_{BOOST} < 1.3V), the DPM duty cycles the transmitter based on available energy. In "red" (V_{BOOST} < 1.1V), the transmitter, accelerator blocks, and front-end amplifiers are clock- and power-gated. Figure 17.4.3 shows the measured closed-loop DPM cycling through the three modes as the boost converter input is swept from 250mV to 20mV and back. Since NOPs are common in biosignal processing, the DPM clock-gates internally to save energy during stalls (2.75pJ/op and 0.7pJ/NOP).

Four subthreshold accelerators, controlled by the DPM, reduce computation delay and increase energy efficiency (Fig. 17.4.4) compared to the MCU for frequently-used functions. A programmable (max 30 taps/band), four-band FIR (384nW at 0.5V and 200kHz) and envelope detector (3.5nW) extract biosignal band energy. An R-R interval extraction and AFib diagnostic block (242nW) determines if an AFib event has occurred [2]. An 8b MCU (242nW) [3] acts as an accelerator for programmable signal processing. Figure 17.4.4 shows the flexibility of this subsystem for processing through the MCU, fully custom processing with accelerators, or a mixed approach. Figure 17.4.4 also shows 3 transmission options to reduce energy. The 4kB data SRAM is controlled by a DMA for efficient memory access, which supports buffering for burst-mode transmissions. The MCU and DPM share instructions from the 1.5kB instruction memory, which includes 90 12b ROM instructions for booting to a default mode from a power down state. Our frequency-multiplying transmitter architecture consumes 160µW when transmitting at its maximum data rate of 200kbps [4]. In raw-data mode, the transmitter operates at a 100% duty-cycle, while the R-R extraction mode reduces the duty cycle and average transmitter power consumption to 0.013% and 190nW, respectively.

An ECG experiment was performed on a healthy human subject. First, the chip was set to ECG raw data mode (consuming 397µW from the 1.35V V_{BOOST} node) (Fig 17.4.5, top). Data was transmitted to a TI CC1101 receiver. The reconstructed ECG (dashed) closely matched the actual ECG. Next, the chip used the on-chip R-R interval extractor to transmit measured heartrate operating from a 30mV supply voltage (Fig. 17.4.5, bottom). Every 5s, V_{BOOST} is sampled to check for sufficient energy, in which case the crystal oscillator is enabled for 20ms before the TX transmission (650µs including turn-on time and transmitting 24b). In AFib detection mode, the R-R and AFib accelerators enable the TX and transmit the last 8 beats of raw ECG (buffered in the data memory) only when a rare AFib event occurs. The total chip power in the R-R/AFib modes is 19µW. A performance comparison is presented in Fig. 17.4.6. To the best of our knowledge, this system has lower power, lower minimum supply voltage (30mV), and more complete system integration than all other reported wireless BASN SoCs. This work presents the first wireless biosignal acquisition chip (Fig. 17.4.7) powered solely from a thermoelectric harvester and/or RF power with integrated supply regulation, AFE, power management, DSP, and TX.

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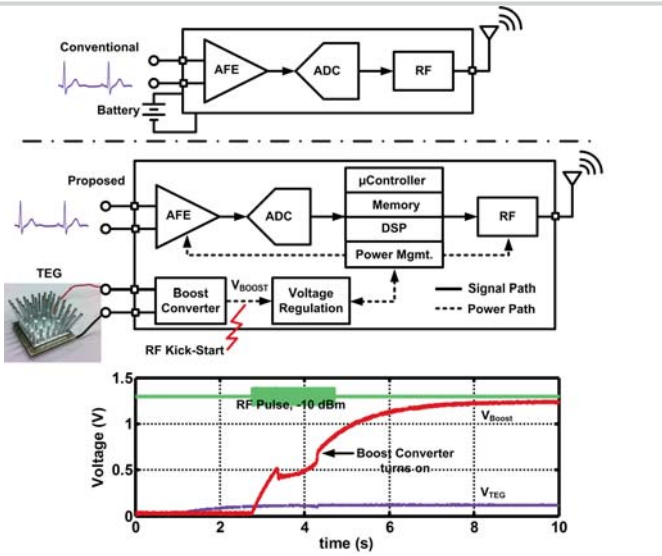

Figure 17.4.1: Motivation of the proposed work and measured RF kick-start of boost converter

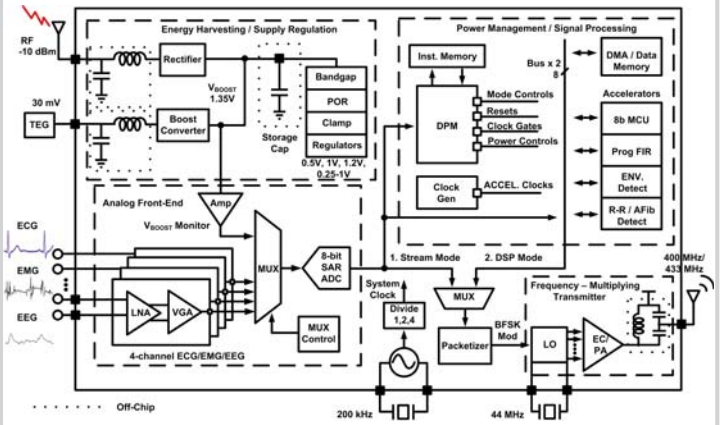

Figure 17.4.2: System block diagram of the BASN SoC.

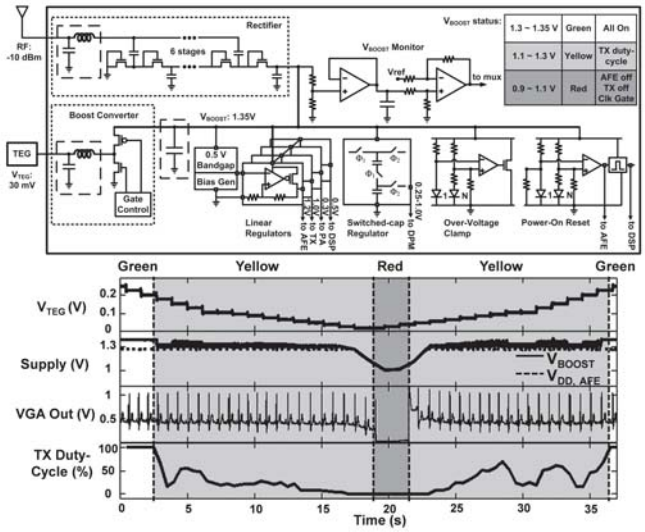

Figure 17.4.3: Energy harvesting / supply regulation circuit and measured closed-loop power management response.

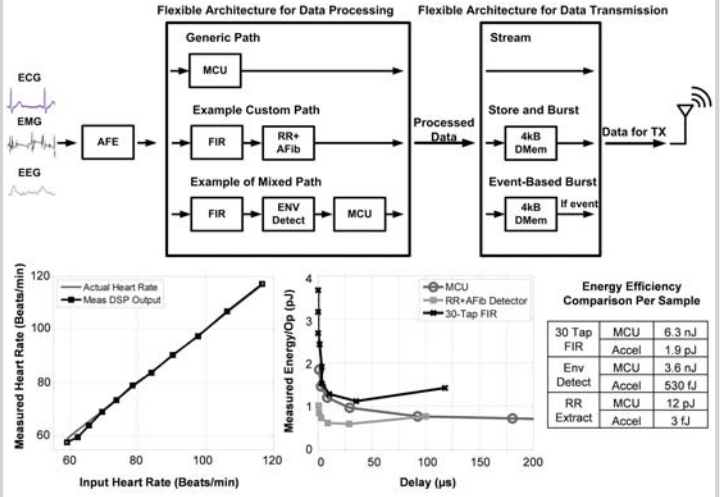

Figure 17.4.4: Digital computation and measured results.

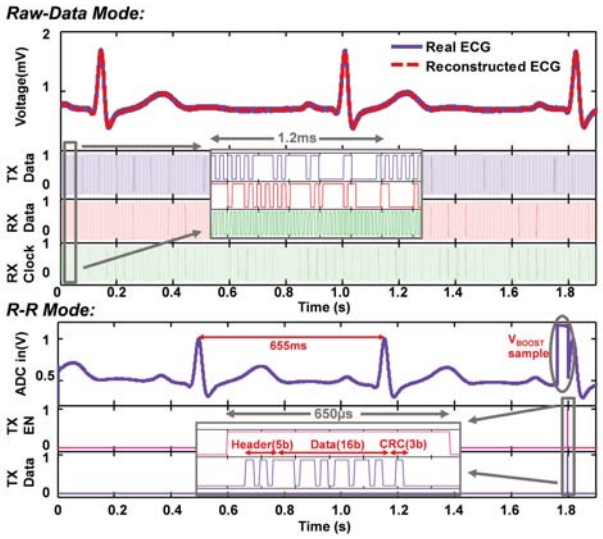

Figure 17.4.5: Measured system performance in raw-data (397µW) and R-R Extraction Modes (19µW, powered from a 30mV supply).

	This Work	Kim (VLSI'11)	Rai (ISSCC'09)	Verma (JSSC'10)	Yan (JSSC'11)	Chen (ISSCC'10)
Sensors	ECG, EMG, EEG	ECG	Neural, ECG, EMG, EEG	EEG	ECG, TIV	Temp, Pressure
Supply Voltage	30mV, -10dBm	1.2V	1V	1V	1.2V	0.4V/0.5V
E Harvesting	Thermal, RF	×	×	×	×	Solar
Supply Reg.	✓	×	×	×	×	✓
AFE	4-channel	3-channel	1-channel	18-channel	4-channel	N/A
Power Mgmt.	DPM, Clock gating, Power gating	Clock gating	×	×	×	Power gating
Gen. Purp. MCU	1.5 pJ/Instr @ 200kHz (8b RISC ISA)	×	×	×	×	28.9pJ/Instr @ 73kHz (32b CORTEX-M3)
Accelerators	Programmable FIR, AFIB, MCU, Envelope Detector, DMA, Packetizer	ASIC DSP (4x SIMD), FIR, Encryption, DMA	×	ASIC DSP	FIR, Packetizer, Compression	×
Memory	5.5kB (0.3V-0.7V)	42kB (1.2V)	×	×	20kB (1.2V)	5kB (0.4V)
DVS	✓	×	×	×	×	×
Digital Power	2.1µW	~12µW	N/A	2.1µW	500µW	2.1µW (MCU)
TX (datarate)	200kb/s	×	100kb/S	×	1Mbps (on-body link)	×
TX P_{DC} (100% on)	160µW	×	400µW	×	2.8mW	×
TX P_{OUT}	-18.5dBm	×	-16dBm	×	-6dBm	×
TX band	402 / 433 MHz	×	402 / 433 MHz	×	20-40 MHz	×
Total Chip Power	19µW	31.1µW	500µW	77.1µW	2.4mW	7.7µW
Note on Total Power (includes):	1-channel AFE, 8b ADC, DSP (R-R extraction), and TX duty-cycled at 0.013%	AFE, 12b ADC, DSP (heart beat detection)	1-channel AFE, 8b ADC, and streaming TX with 100% duty-cycle	18-channel AFE, 12b ADC, and DSP (EEG feature extraction)	4-channel AFE, 10b ADC, DSP (data compression, FIR), SRAM, TX at 5% duty cycle	Data acquisition, DSP (DFT), storage in SRAM
Technology	130nm	180nm	130nm	180nm	180nm	180nm

Figure 17.4.6: Comparison with other integrated sensing SoCs.

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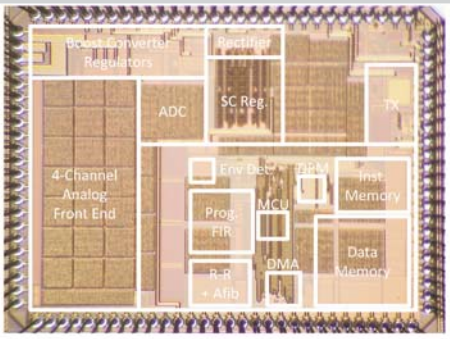

Energy Harvesting		Supply Regulation		AFE (1 CH, ADC, logic)		DSP		TX	
V_{in}	30mV	V_{unreg}	> 1.25V	Current	4µA	Op. range	0.3-1.2V	Current	280µA
Kick-start	RF @ -10dBm	$I_{quiescent}$	3µA	Supply	1.2V	MCU E/op @0.5V	1.5pJ	Supply	1V (LO) 0.5V (PA)
V_{out}	1.35 V	$V_{analog,digital}$	0.5V, 1V, 1.2V,	Gain	40-78dB	IMEM E/rd/Inst	1.0pJ	Data-rate	200kbps
Efficiency	38%	V_{PA} V_{DVS}	0.3-0.5V 0.25-1V	$V_{ni,rms}$	< 2µV_{rms}	FIR FOM*	0.27	E/b	0.8nJ/b
System Power				Bandwidth	0-320Hz	AFib E/sample @0.5 V	6pJ	Output Power	-18.5dBm
Current	14µA (R-R) (0.013% TX duty cycle)		294µA (Raw-data) (100% TX duty cycle)	CMRR	> 70dB	Env E/sample @0.5V	.53 pJ	Band	400MHz MICS/ 433MHz ISM
Supply	1.35 V					Sub-V_t DVS: 0.3V to 0.6V	2kHz-1.7MHz	Modulation	BFSK

FIR FOM*: Power(nW) / frequency(MHz) / # of taps / input bit length / coefficient bit length

Figure 17.4.7: Die photo and SoC performance summary.

978-1-4673-0377-4/12/$31.00