



Analyzing Static and Dynamic Write Margin for Nanometer SRAMs

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Overview

- Motivation and Background.
- A Key Insight.
- Dynamic write-ability analysis.
- Static vs. Dynamic measures.
- Conclusions.

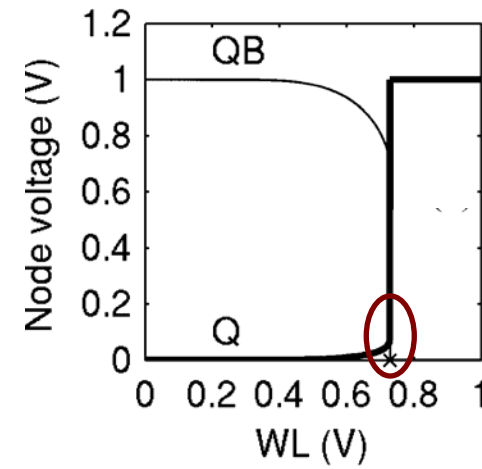
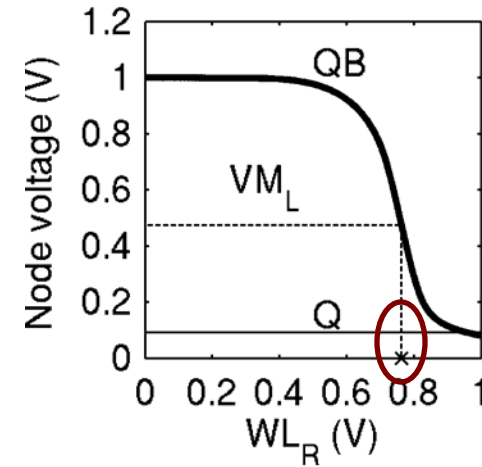
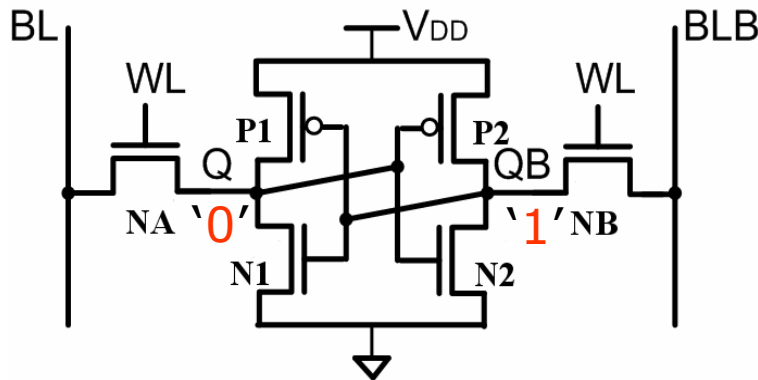


Motivation

- \uparrow varn. \Rightarrow \downarrow noise margins.
- Static metrics
 - Easy to measure
 - Ignore time
 - Pessimistic
 - Best metric?
- Better VCC_{\min} estimation \Rightarrow dynamic write-ability metric reqd.

Background: Static Approaches

WL Sweep 1 (V_{WL_R})



$WM = V_{DD} - WL$

WL Sweep 2 (V_{WL})

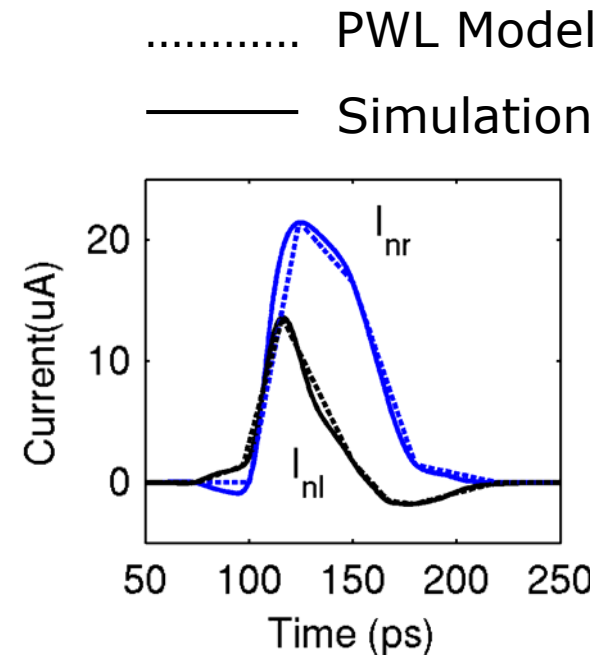
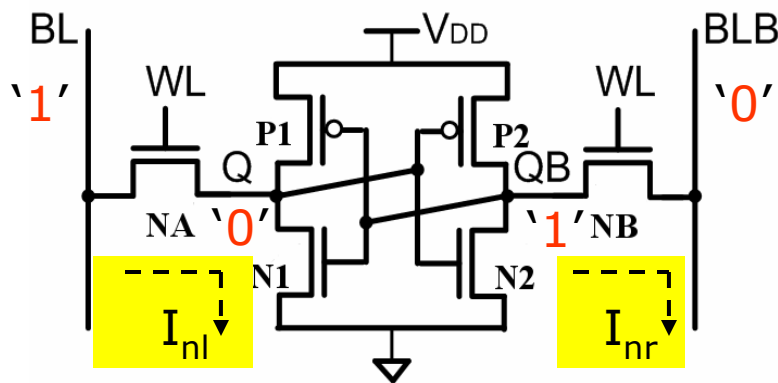


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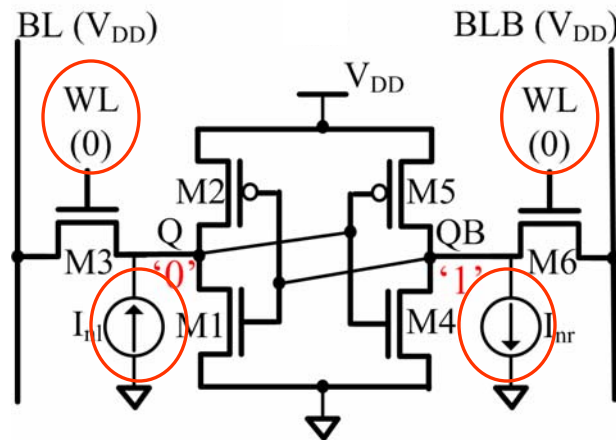
SRAM Write Operation

Currents look like noise pulses injected into the cell through access NFETs

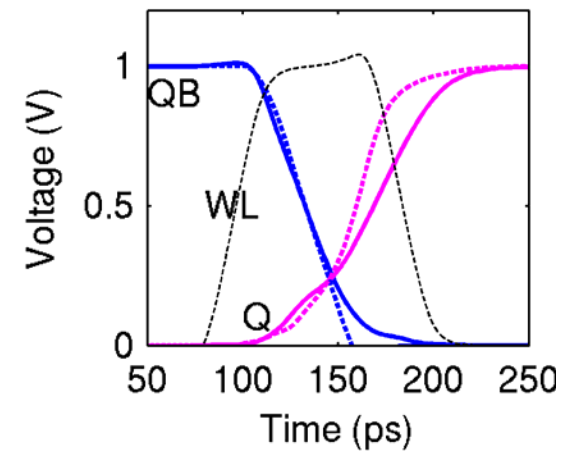


The current can be modeled by nearly triangular PWL pulse

SRAM Write Operation



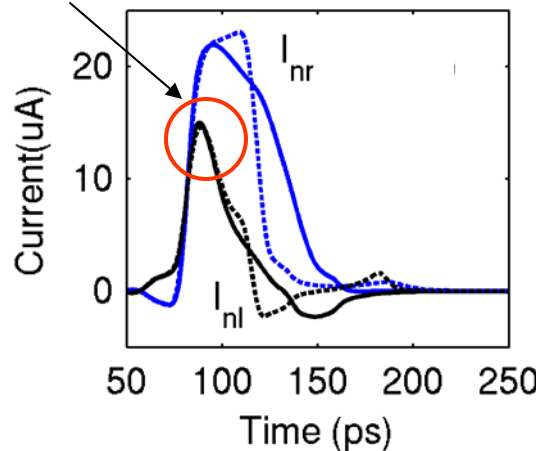
..... Current noise Model
—— Write Simulation



Key Insight: Current noise model of the write operation closely resembles actual write operation

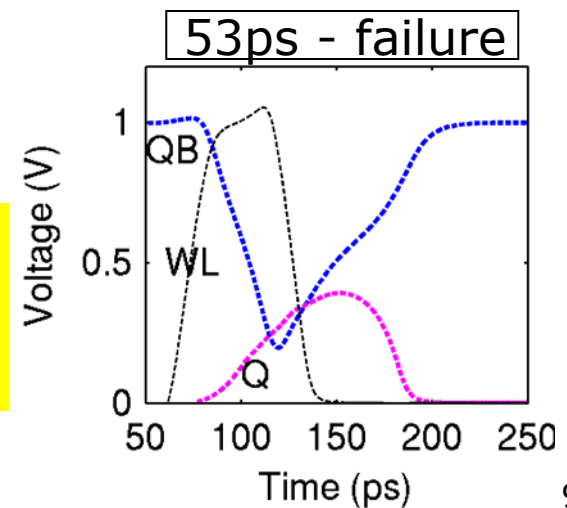
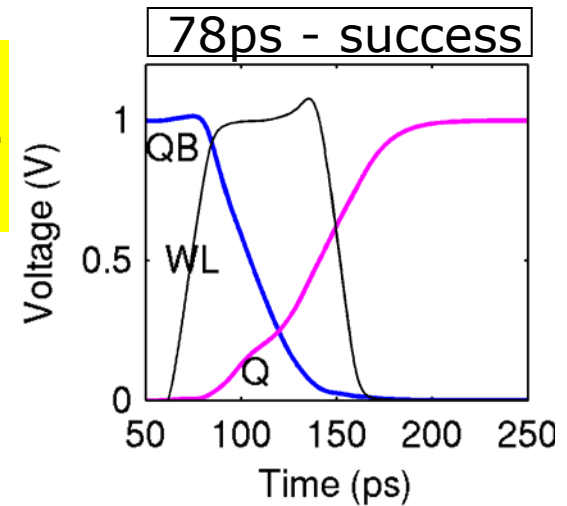
Dependency on WL pulse width

Same current amplitude



Longer WL duration
⇒ wider current pulse
⇒ write success

Insufficient WL duration
⇒ shorter current pulse
⇒ write failure



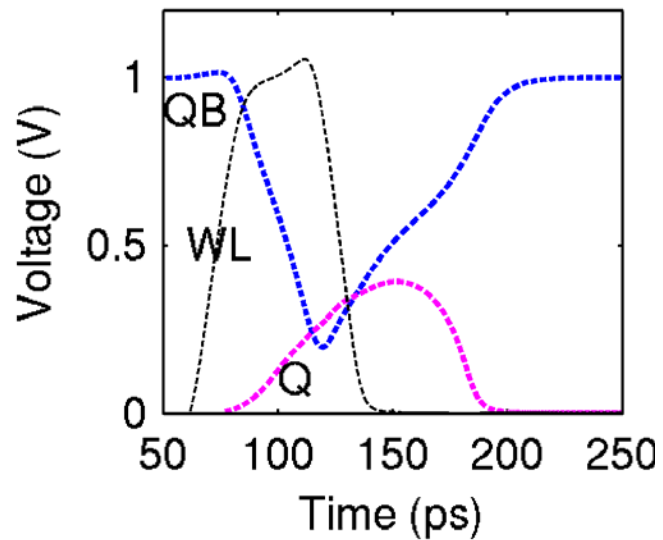


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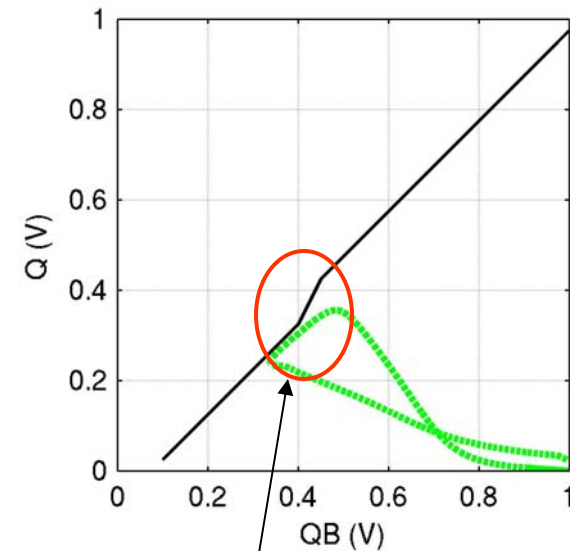
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Dynamic write-ability analysis

$$T_{WL} = T_{CRIT} - 1ps$$

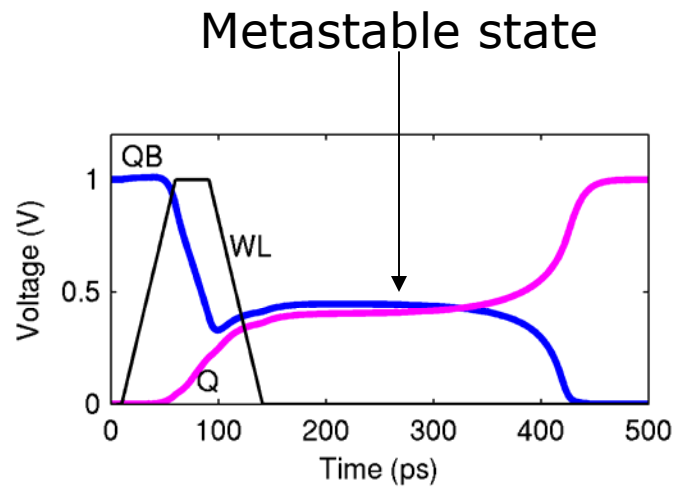


Separatrix = boundary
between attraction
regions

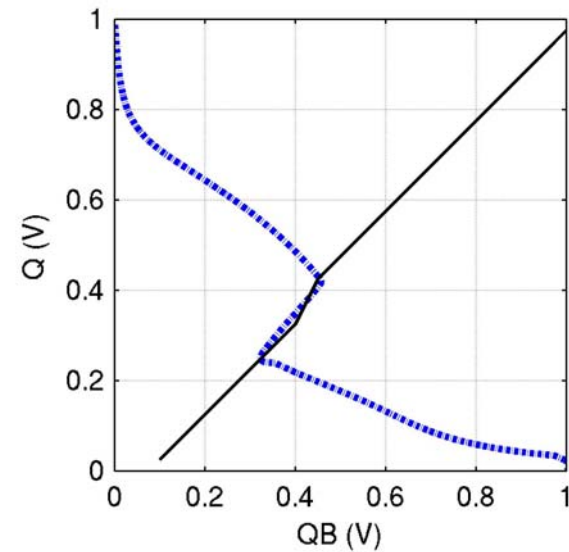


Variation skews
separatrix

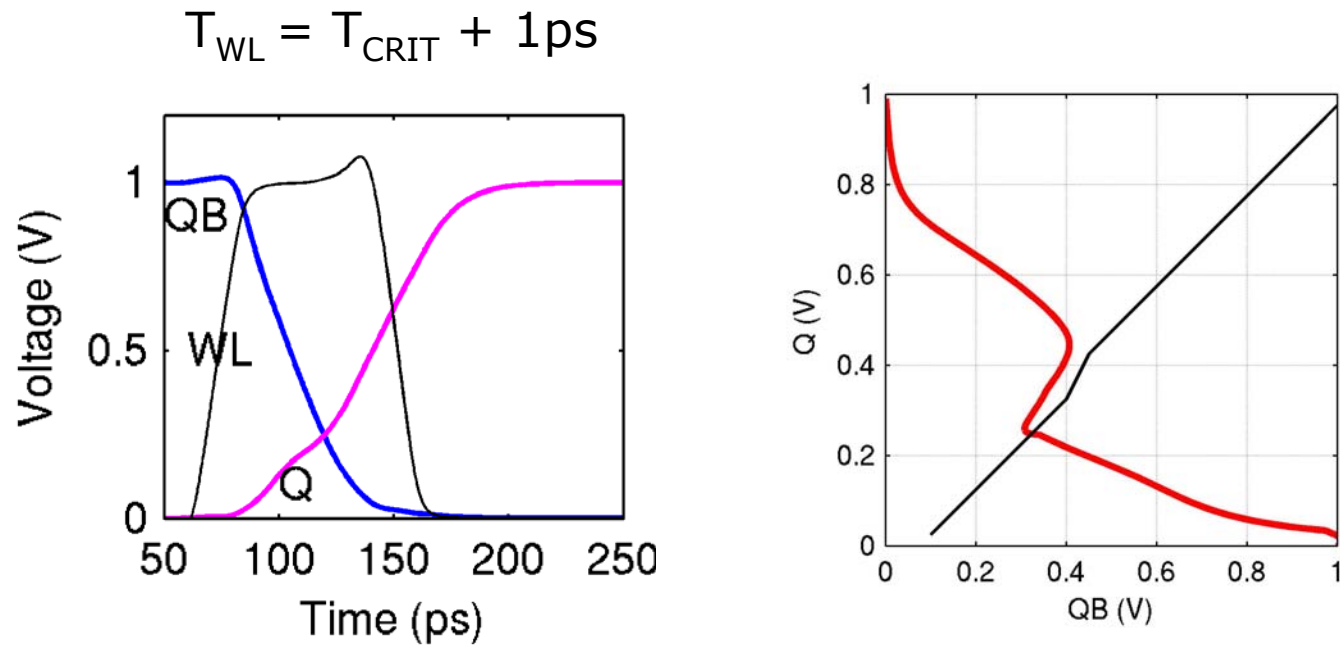
Dynamic write-ability analysis



$$T_{WL} = T_{CRIT}$$



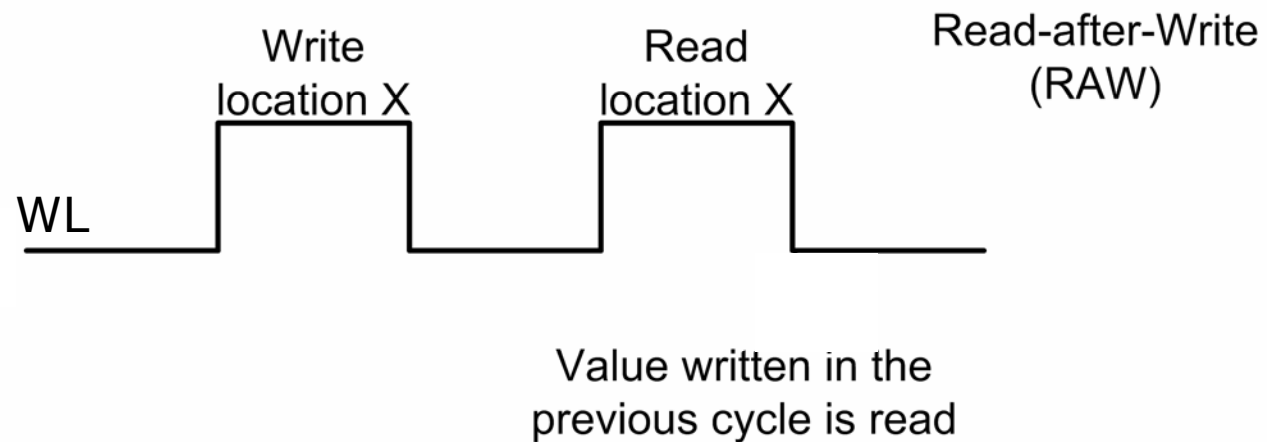
Dynamic write-ability analysis



T_{CRIT} = WL pulse width when the cell just flips

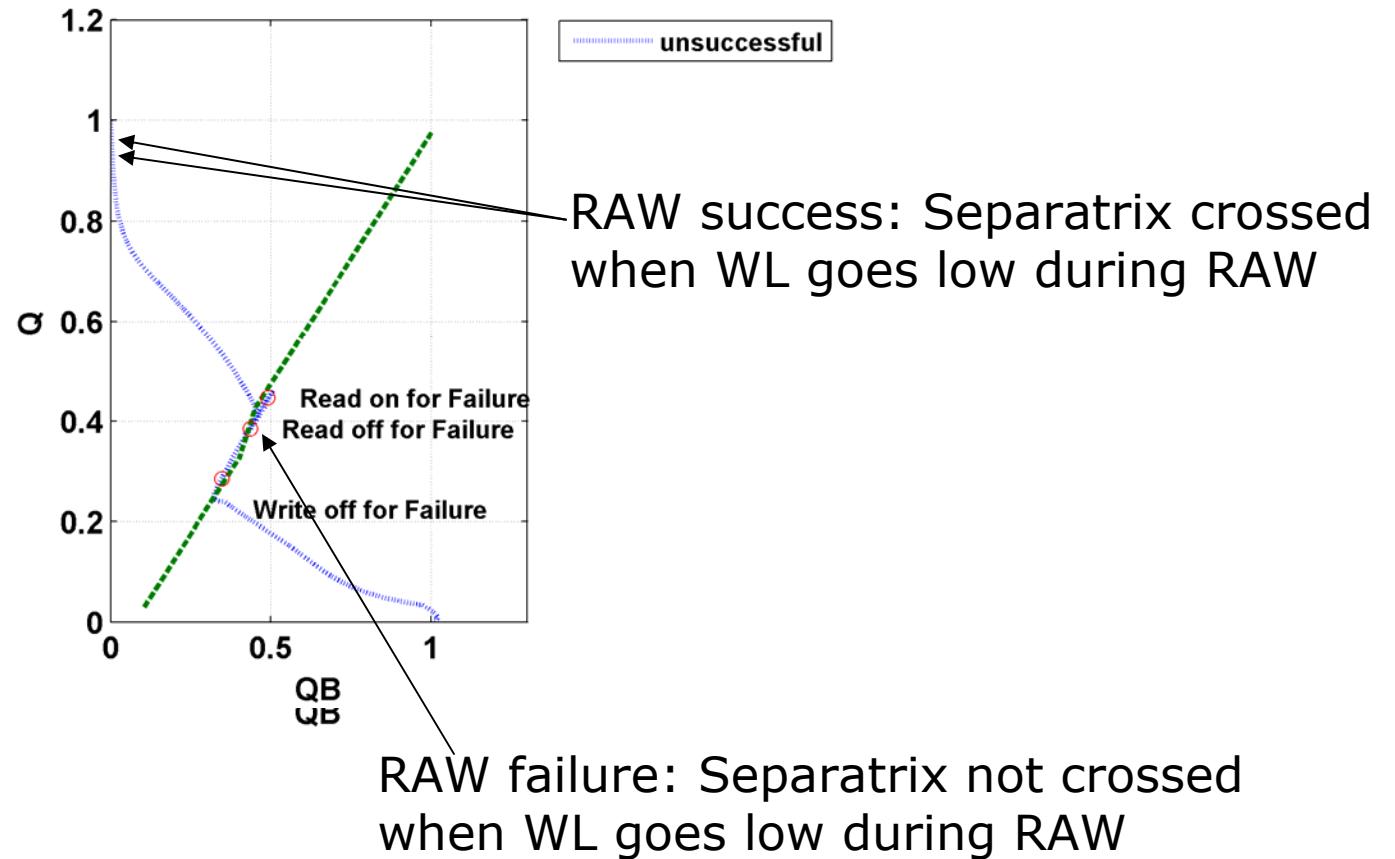
Write Failure definition

- Cell eventually flips
- Correct Read-after-write (RAW)

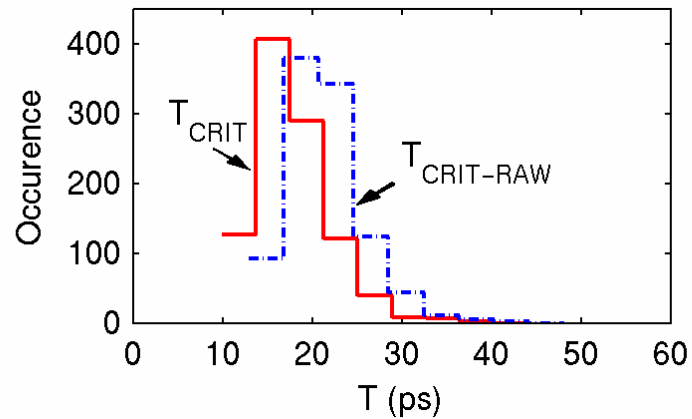


$$T_{\text{CRIT-RAW}} = \min. T_{\text{WL}} \text{ needed for successful RAW.}$$

Dynamic write-ability analysis: RAW



T_{CRIT} VS. $T_{\text{CRIT-RAW}}$



- Similar distributions.
- T_{CRIT} simulation easier.
- High-speed SRAM $\Rightarrow T_{\text{CRIT-RAW}}$
- Slower SRAMs $\Rightarrow T_{\text{CRIT}}$



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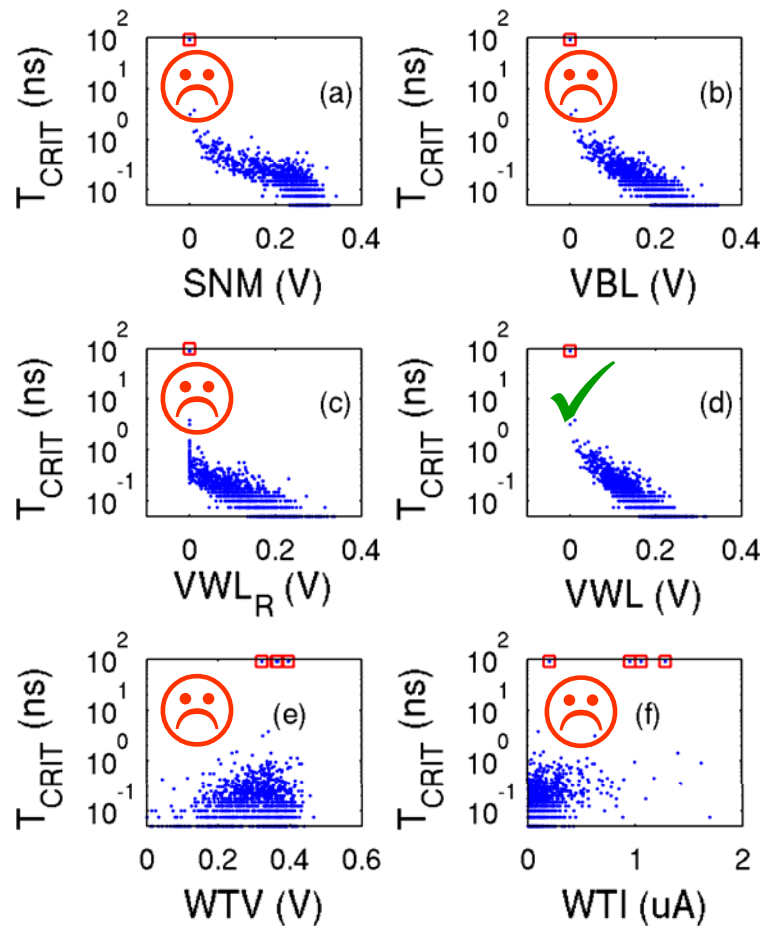
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Correlation with Access transistor

	T_{CRIT}	Least Sqs.	BL sweep	WL sweep 1	WL sweep 2	N-curve	
Corr. Coeff.	0.6	-0.54	-0.61	-0.60	-0.65	-0.15	-0.03

N-curve metrics poorly correlated with ΔV_T of Access FET

Correlation with static metrics



Correlations at
VDD = 0.6 V

Can use static metric to
prescreen and follow up
with dynamic metric

Best correlated static
metric: WL sweep 2



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Conclusions

- Modeled write operation as current noise pulse.
- Used Separatrix and T_{CRIT} for dynamic write-ability.
- Studied correlation between static and dynamic metrics.
- Found most correlated static metric.



Thank You

- Thank you for your attention.
- This work was supported by the MARCO/DARPA Focus Research Center for Circuit and Systems Solutions(C2S2) and by the SRC.
- Any Questions?