Analyzing Static and Dynamic Write Margin for Nanometer SRAMs

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Overview

- Motivation and Background.
- A Key Insight.
- Dynamic write-ability analysis.
- Static vs. Dynamic measures.
- Conclusions.
Motivation

- ↑ varn. ⇒ ↓ noise margins.
- Static metrics
  - Easy to measure
  - Ignore time
  - Pessimistic
  - Best metric?
- Better $VCC_{\text{min}}$ estimation ⇒ dynamic write-ability metric reqd.
Background: Static Approaches

Least Squares (SNM)

BL Sweep (VBL)

N-Curve (WTV, WTI)
Background: Static Approaches

WL Sweep 1 (VWL_R)

WL Sweep 2 (VWL)

WM = VDD - WL
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SRAM Write Operation

Currents look like noise pulses injected into the cell through access NFETs

The current can be modeled by nearly triangular PWL pulse
SRAM Write Operation

Key Insight: Current noise model of the write operation closely resembles actual write operation
Dependency on WL pulse width

Longer WL duration ⇒ wider current pulse ⇒ write success

Insufficient WL duration ⇒ shorter current pulse ⇒ write failure
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Dynamic write-ability analysis

\[ T_{WL} = T_{CRIT} - 1\text{ps} \]

Separatrix = boundary between attraction regions

Variation skews separatrix
Dynamic write-ability analysis

\[ T_{\text{WL}} = T_{\text{CRIT}} \]
Dynamic write-ability analysis

\[ T_{WL} = T_{CRIT} + 1\text{ps} \]

\[ T_{CRIT} = \text{WL pulse width when the cell just flips} \]
Write Failure definition

• Cell eventually flips
• Correct Read-after-write (RAW)

\[ T_{\text{CRIT-RAW}} = \min. T_{\text{WL}} \text{ needed for successful RAW.} \]
Dynamic write-ability analysis: RAW

RAW success: Separatrix crossed when WL goes low during RAW

RAW failure: Separatrix not crossed when WL goes low during RAW
$T_{\text{CRIT}}$ vs. $T_{\text{CRIT-RAW}}$

- Similar distributions.
- $T_{\text{CRIT}}$ simulation easier.
- High-speed SRAM $\Rightarrow T_{\text{CRIT-RAW}}$
- Slower SRAMs $\Rightarrow T_{\text{CRIT}}$
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Correlation with Access transistor

<table>
<thead>
<tr>
<th></th>
<th>$T_{CRIT}$</th>
<th>Least Sq.</th>
<th>BL sweep</th>
<th>WL sweep 1</th>
<th>WL sweep 2</th>
<th>N-curve</th>
</tr>
</thead>
<tbody>
<tr>
<td>Corr. Coeff.</td>
<td>0.6</td>
<td>-0.54</td>
<td>-0.61</td>
<td>-0.60</td>
<td>-0.65</td>
<td>-0.15</td>
</tr>
</tbody>
</table>

N-curve metrics poorly correlated with $\Delta V_T$ of Access FET
Correlation with static metrics

Correlations at VDD = 0.6 V

Can use static metric to prescreen and follow up with dynamic metric

Best correlated static metric: WL sweep 2
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Conclusions

- Modeled write operation as current noise pulse.
- Used Separatrix and $T_{CRIT}$ for dynamic write-ability.
- Studied correlation between static and dynamic metrics.
- Found most correlated static metric.
Thank You

- Thank you for your attention.
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- Any Questions?