Minimizing Offset for Latching Voltage-Mode Sense Amplifiers for Sub-threshold Operation

(A Digital Designer's View)

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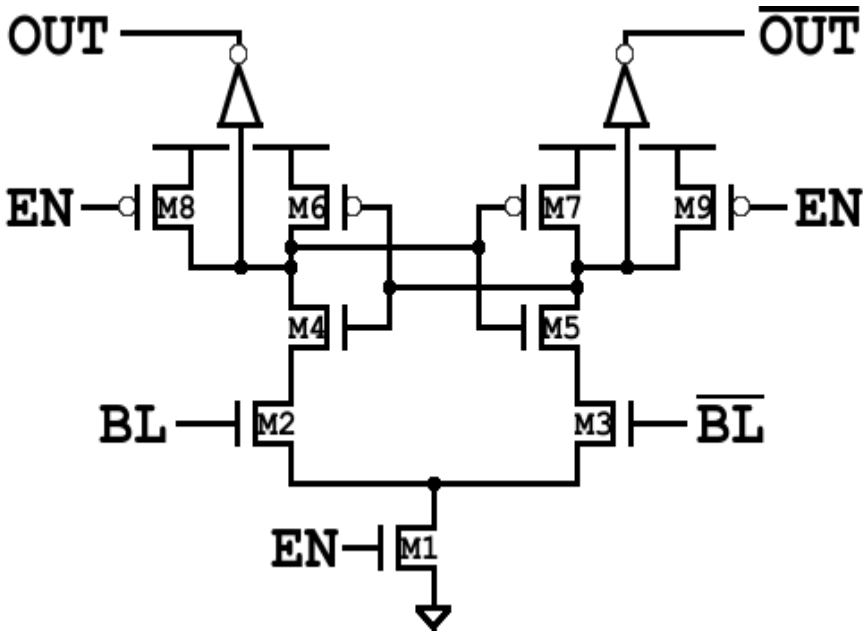
Sub-V_T Sense Amps: Outline

- **Sense Amplifiers in Sub-V_T**
- Intrinsic Offset
- Design Methodology
- Design Examples
- Conclusion

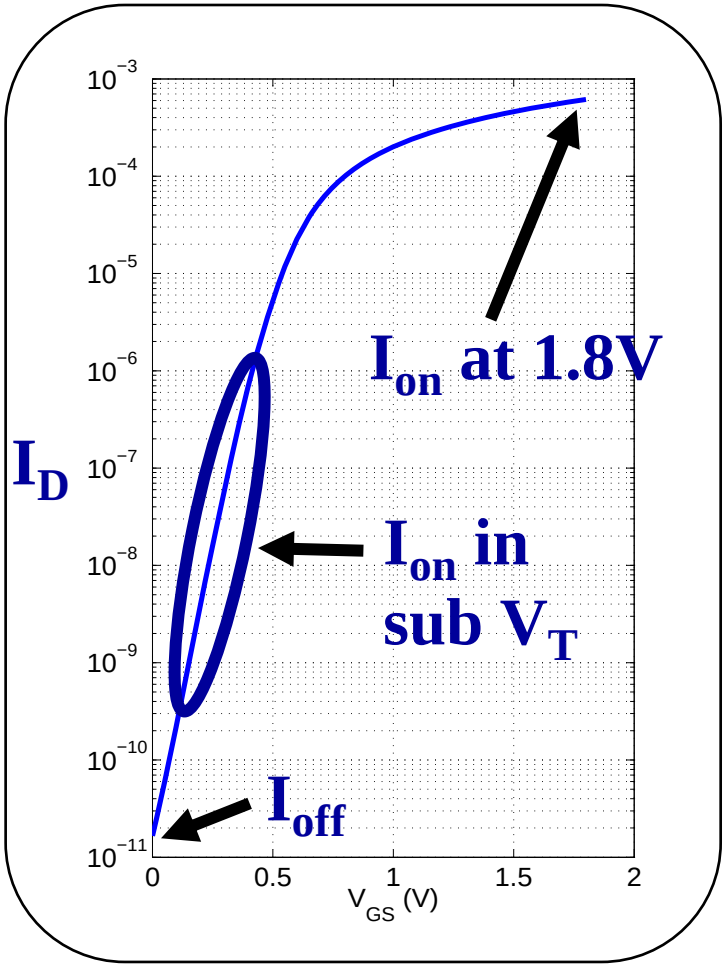
Sense Amps

- Sense Amplifier – circuit component that compares two DC voltages and latches a digital value based on which input is larger.

- Used in SRAM, DRAM, ADCs, Interconnect, etc.
- Tricky in Sub-V_T



Sub-threshold Operation



- $V_{DD}<V_T$
- Sub-threshold current for I_{ON} and I_{OFF}
- Well-suited for minimum energy or ultra-low power applications

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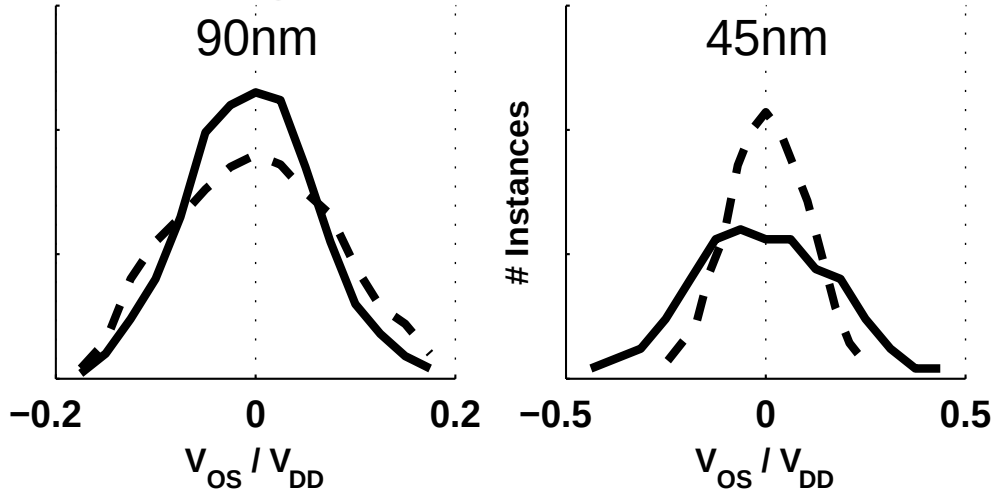
Sub V_T Sense Amps: The Problem

- Sense Amplifier offset voltage: Intrinsic error caused by Process Variations.

- Becomes relatively worse at low V_{DD}, especially in newer technologies!



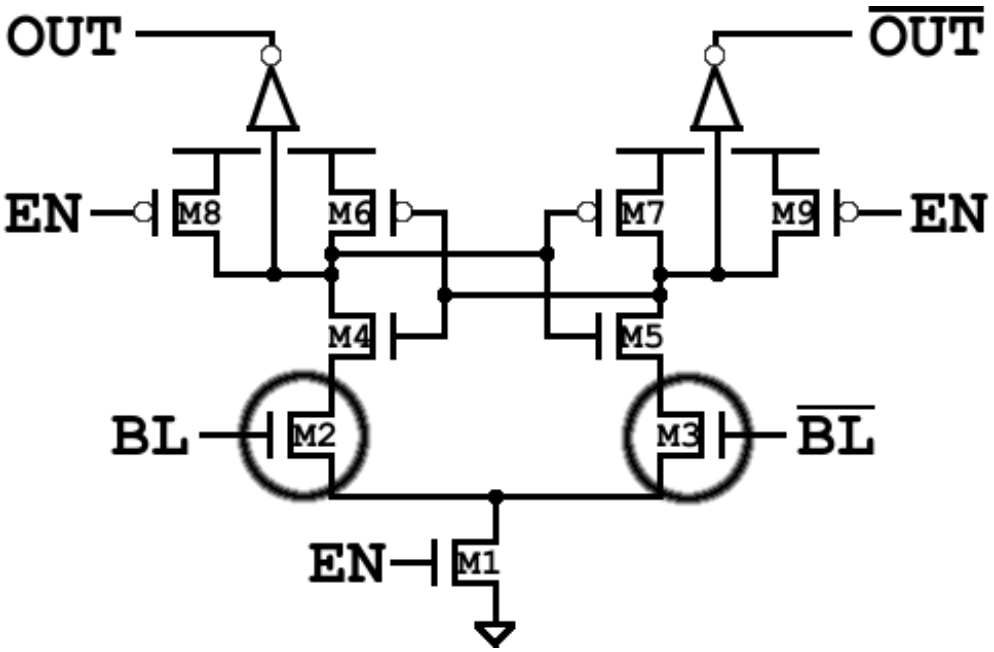
V_{DD}=1V (dashed), 0.4V (solid)

Sub-V_T Sense Amps

- Primary concern: reduce offset
  - Why? More robust and efficient
- Approach: Find sources of offset
  - Develop a model and design methodology.

Sense-Amp Offset – Input Pair

- Offset Contributions from input pair
- Assuming random V_T variation between M2 and M3,
- $V_{OS}=V_{T2}-V_{T3}$.

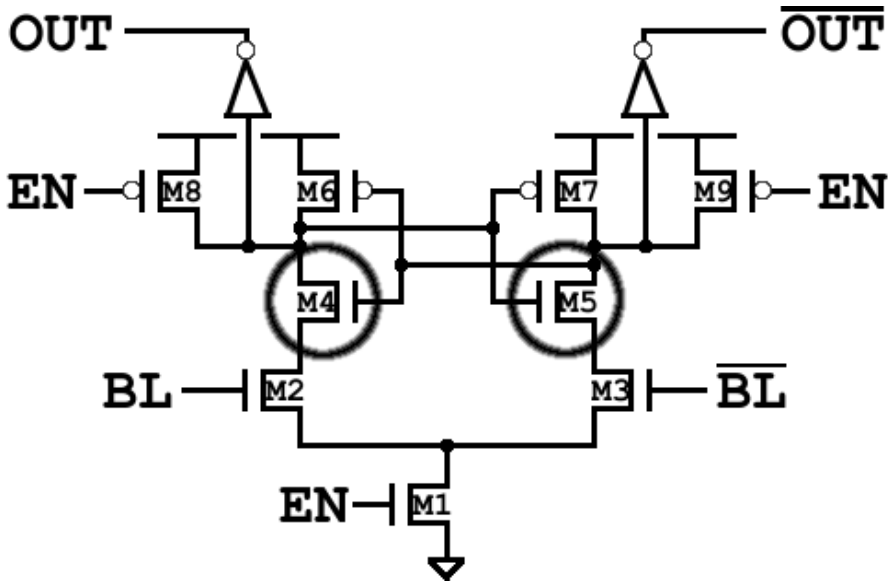


Sense-Amp Offset – Inverter Pair

- Next up: the cross-coupled inverter pair.
- Contribution from PMOS: very small.

- The NMOS pair, however, has a large effect on V_{OS}.

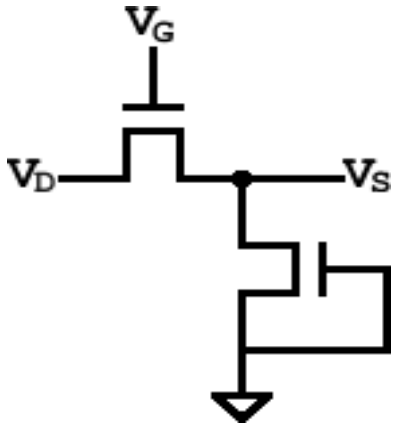
- Analyze during **reset** phase: NMOS acts as a pass-gate

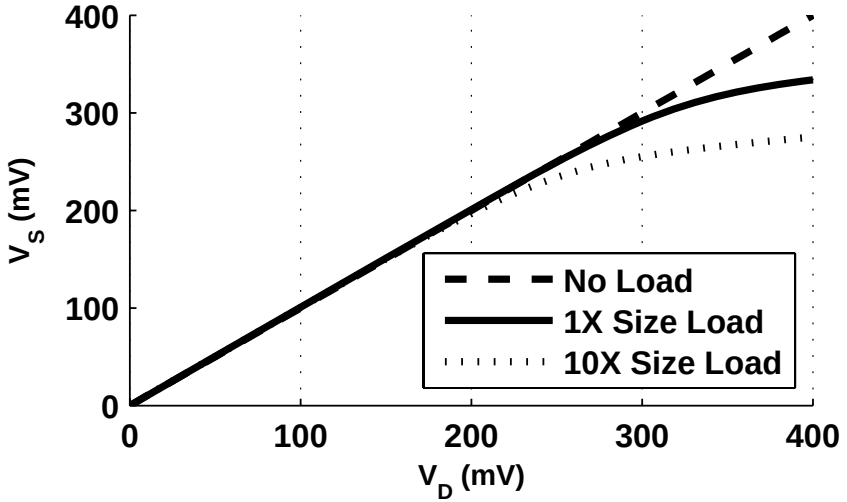


Sub-V_T Pass Gate

- $V_D < V_T \rightarrow$ no V_T drop!
- V_{DS} drop due to leakage/load currents at the source.
- Primarily due to DIBL (Drain-Induced Barrier Lowering).

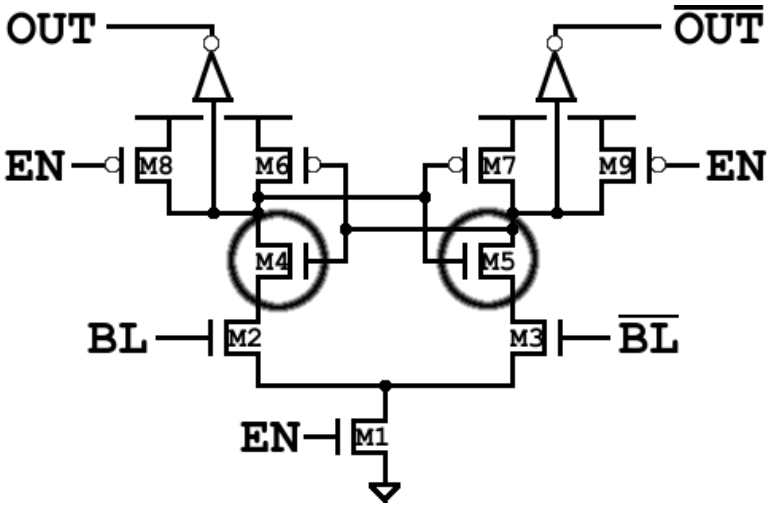
$$V_S \approx \frac{1}{\alpha}(V_G + \eta V_D + S * \log_{10}(W_{PG}/N * W_L))$$

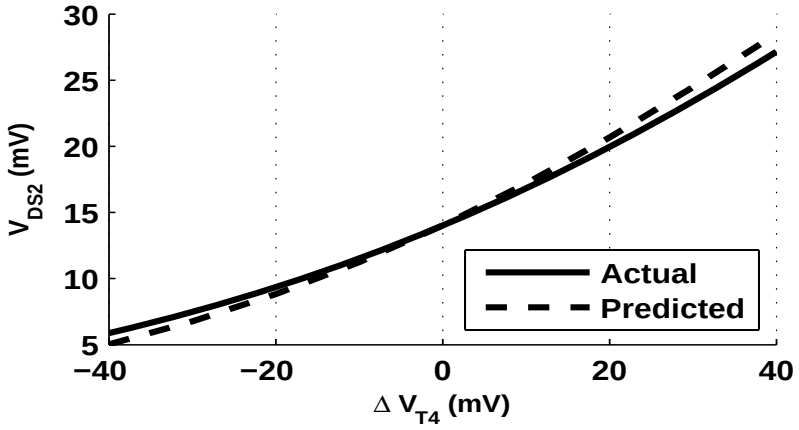




Sense-Amp Offset – Inverter Pair

- So: during reset phase, variations in V_T in M4 & M5 can cause M2 & M3 to be buried further into the Sub-V_T roll-off region due to V_{DS} shifts!

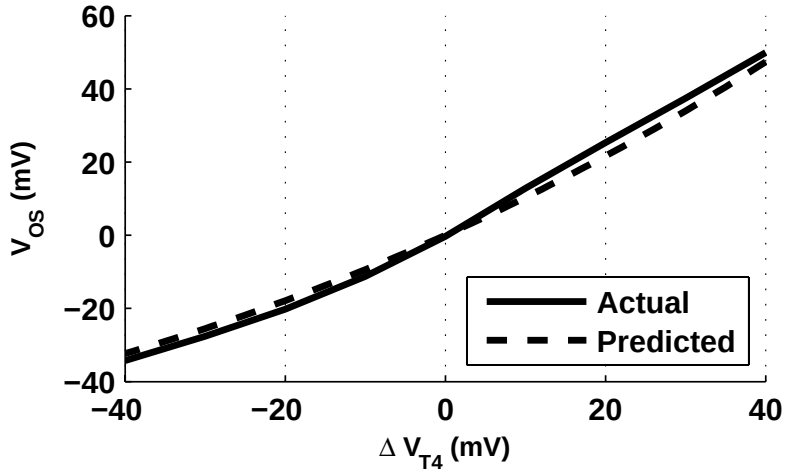




Sense-Amp Offset – Inverter Pair

- Thus, variations in M4 & M5 have just as large an impact on V_{OS} as M2 & M3!

- $V_{OS} \approx (V_{T2}-V_{T3}) + (V_{T4}-V_{T5})$



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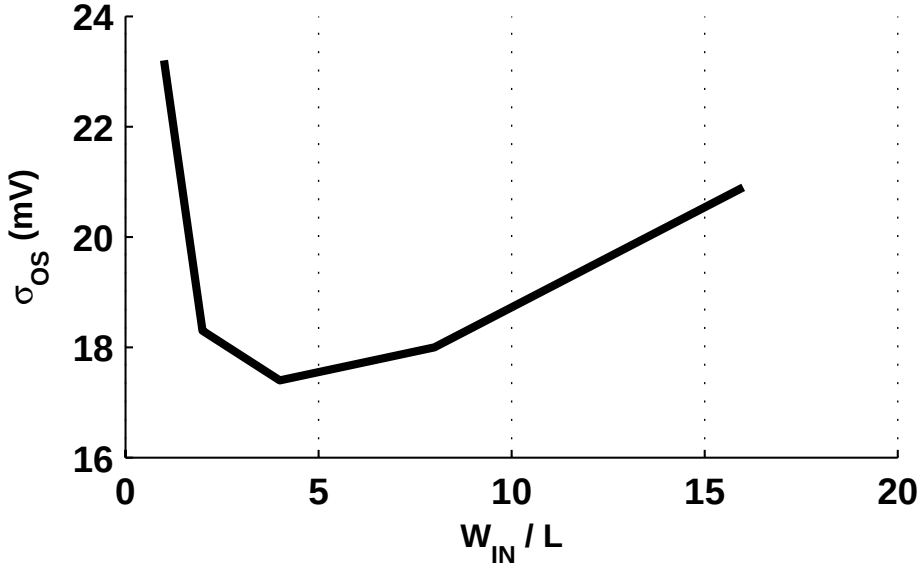
Reducing Offset: Sizing

- Variation in V_T proportional to 1/sqrt(W*L).
- Not true for sub-V_T SA?!
- This is again due to $V_{DS2,3}$ and the roll-off region.
- What if we raise V_{DS} out of this region?



Reducing Offset

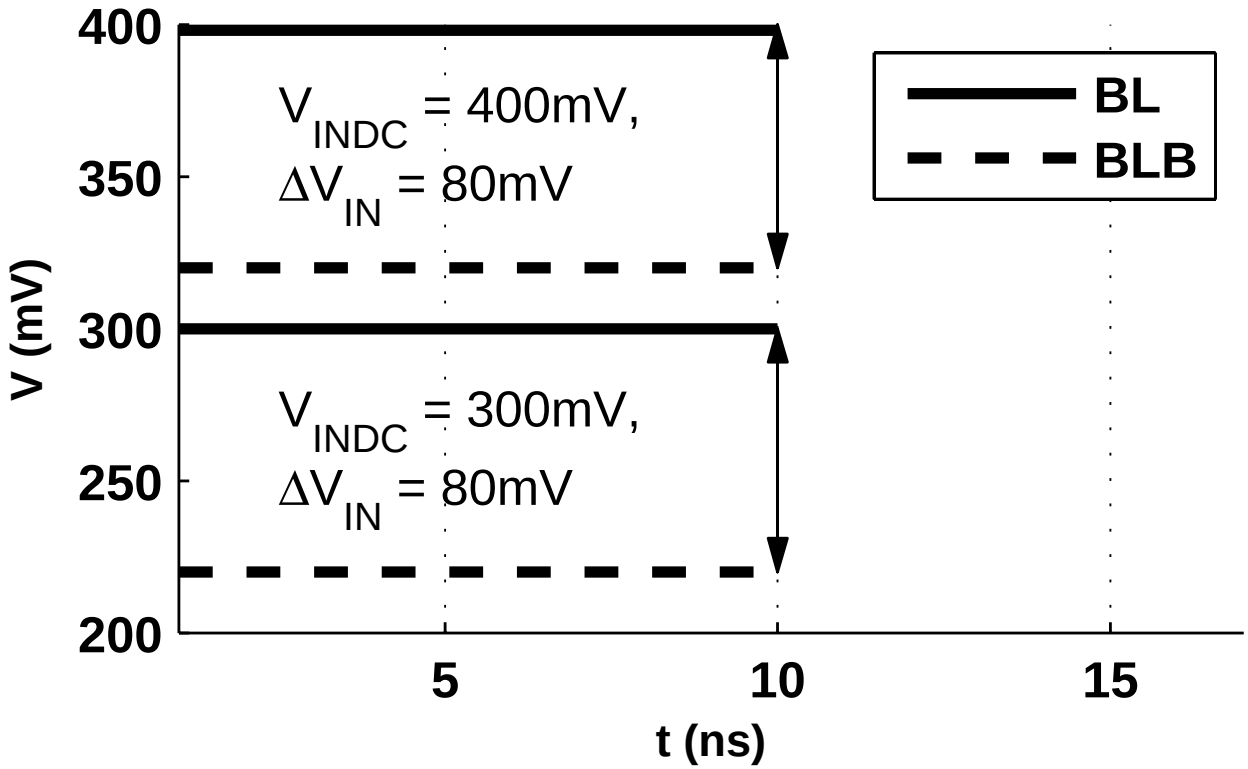
- Looking at the pass-gate DC equation provides an important clue:

$$V_S \approx \frac{1}{\alpha}(V_G + \eta V_D + S * \log_{10}(W_P / N * W_L) + \Delta V_T)$$

- V_G, the voltage at the input pair, is the largest contributor – why not lower that?
- $V_G = V_{INDC} + \Delta V_{IN}$
- Lower V_{INDC} to lower V_G.

What is V_{INDC}?

- V_{INDC} is the DC voltage at inputs before ΔV_{IN} is applied



Reducing Offset: V_{INDC}

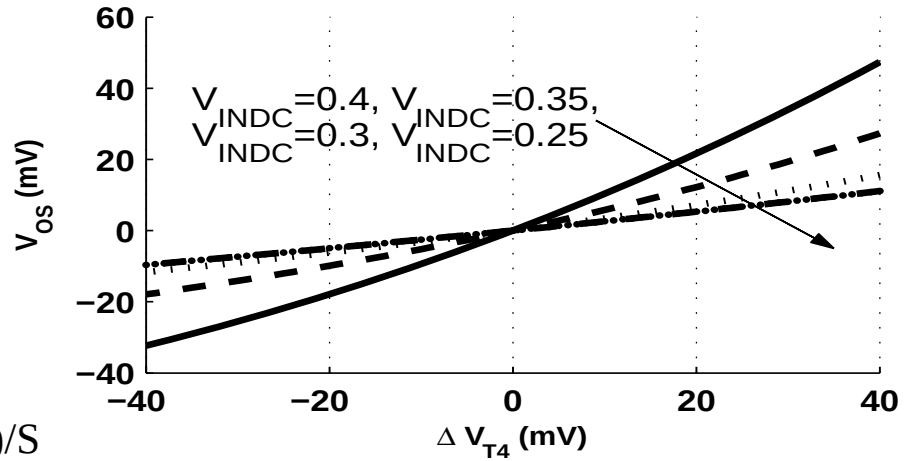
- Lowering V_{INDC} cancels out variation of M4 & M5 by moving $V_{DS2,3}$ out of roll-off region!

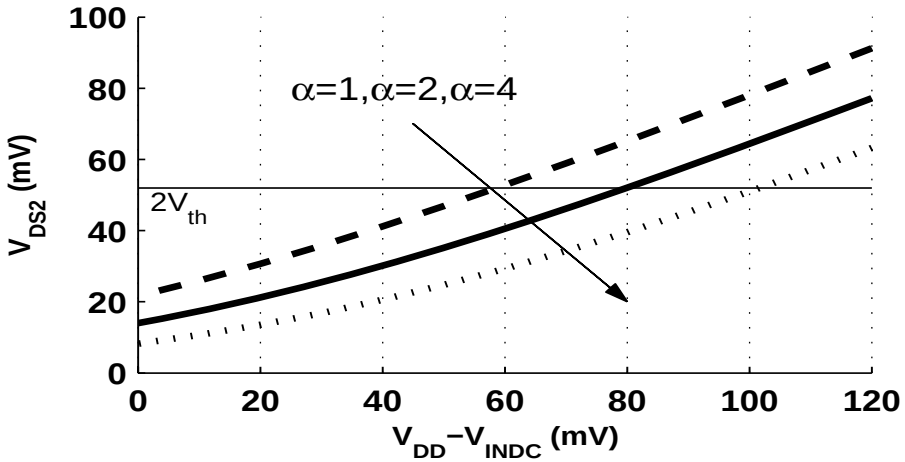
- $V_{OS} \approx (V_{T2}-V_{T3}) + (V_{T4}-V_{T5})*10^{-(V_{DD}-V_{INDC})/S}$

- Note upsizing input-pair counters V_{INDC}:

$$V_{INDC-EFF} = V_{INDC} - s*\log_{10}(\alpha/2)$$

$$\alpha = W_{IN}/W_{INV}$$





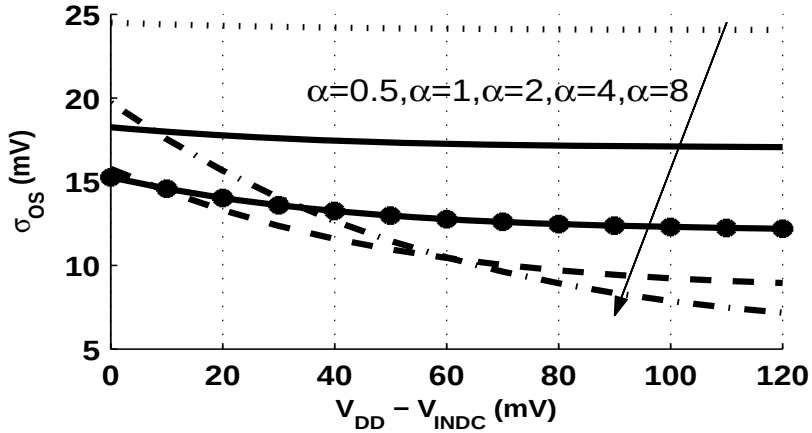
Reducing Offset: Model

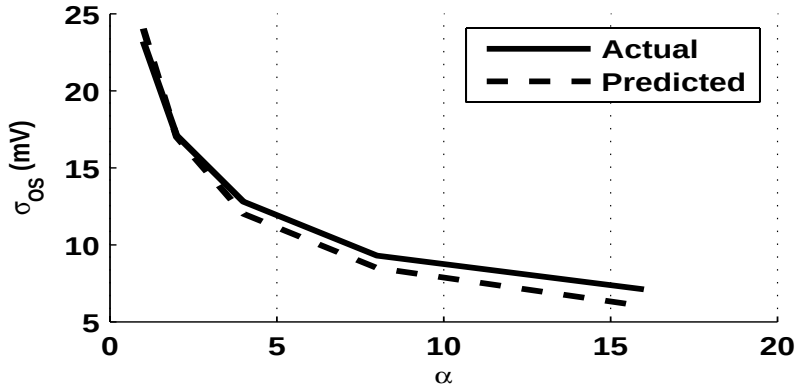
- All together provides a model for standard deviation:

$$\sigma_{OS} \approx \frac{\sigma_N}{\sqrt{W_{IN} * L/2}} \sqrt{1 + \alpha * 10^{-(V_{DD} - V_{INDC-EFF})/S}}$$

- Properly matched V_{INDC} and W_{IN} cancel variation on transistors M4 & M5.

$$\sigma_{OS} \approx \sigma_N / \sqrt{L * W_{IN}/2}$$





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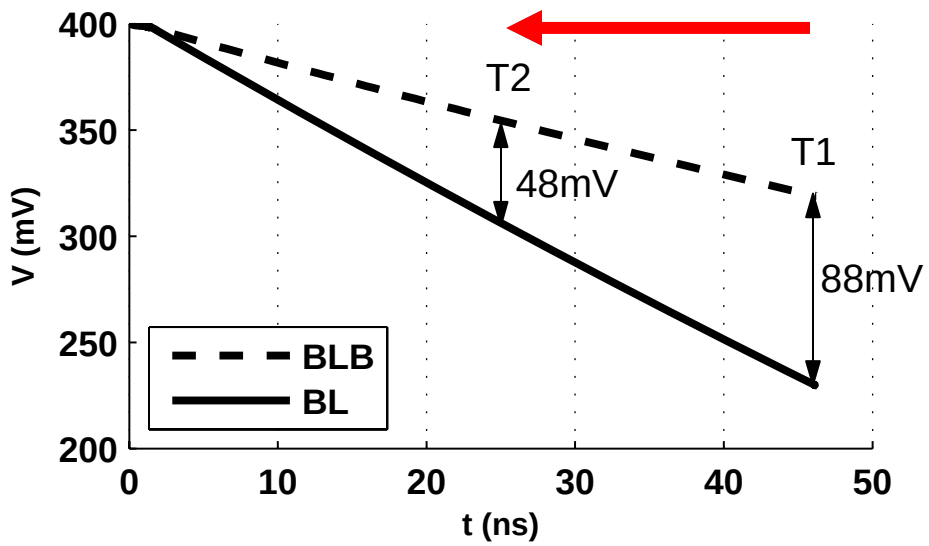
Design Examples - SRAM

- SRAM bitline leakage
  - Requires longer read time for $\Delta V_{BL} > V_{OS}$
- Leakage adjusts V_{INDC} of the sense-amplifier!
  - Both BLs discharge
- Decreases effective offset
  - Shorter read time possible!

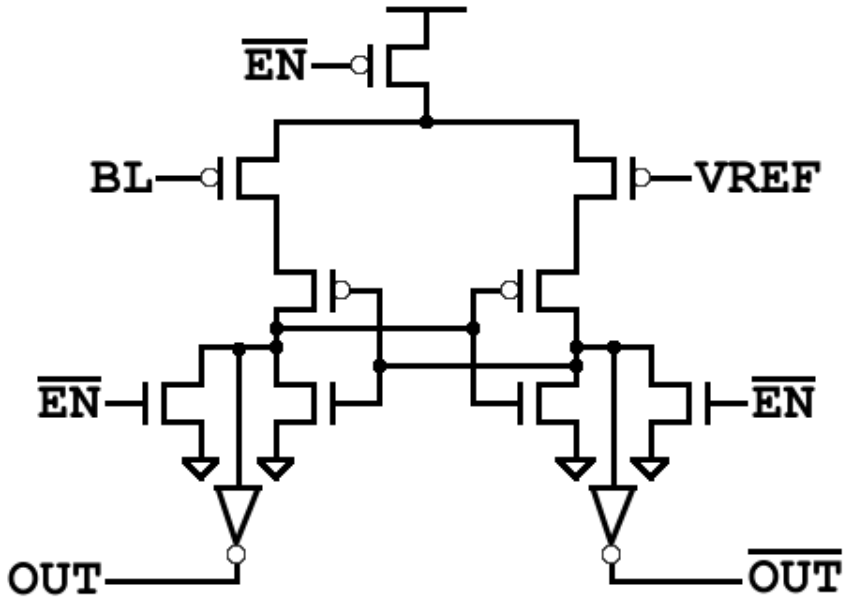
Design Examples - SRAM

- T1 – Trigger if Sense-Amp offset is only measured at V_{INDC}=0.
- T2 – Trigger if V_{INDC} effects are considered on Sense-Amp standard deviation.
- **Read-time is dramatically reduced !!**



Design Examples - Interconnect

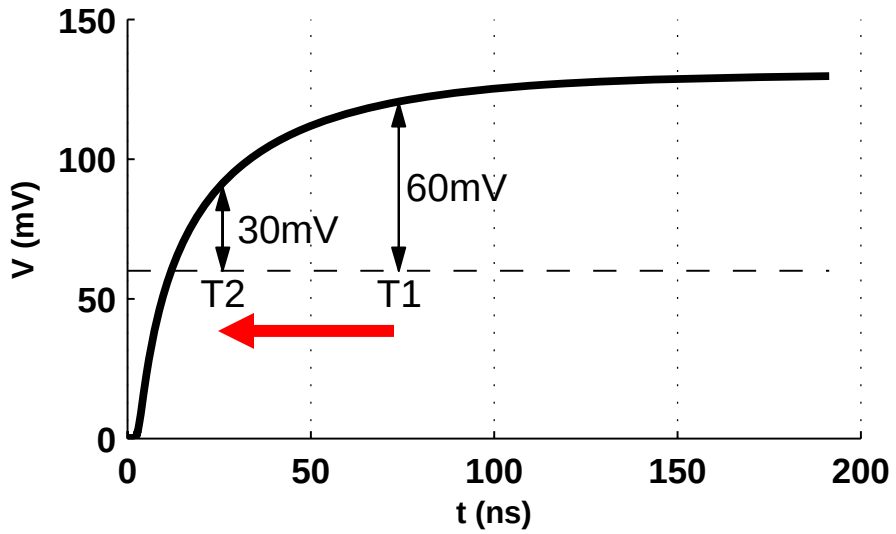
- Low-swing interconnect scheme can be faster and save more power than traditional buffer methods.
- Receiver: Sense-Amp (p-input dual) triggered before signal has finished resolving.
- Input compared to a reference rather than a paired wire to save area.



Low-Swing Receiver

Design Examples - Interconnect

- Pseudo-diff. structure has asymmetrical offset!
- Reading a “0”: V_{INDC}=0.
- Reading a “1”: V_{INDC}=V_{REF} → Pick higher V_{REF} to lower offset
- Delay-time is again dramatically reduced!



Conclusions

- Properly matched V_{INDC} and W_{IN} cancel the effects of variation everywhere except the input pair.
- Our model leads to an efficient design methodology.
- Naturally-occurring V_{INDC} can be harnessed to improve the efficiency of the system.