Analyzing and Modeling Process Balance for Sub-Threshold Circuit Design

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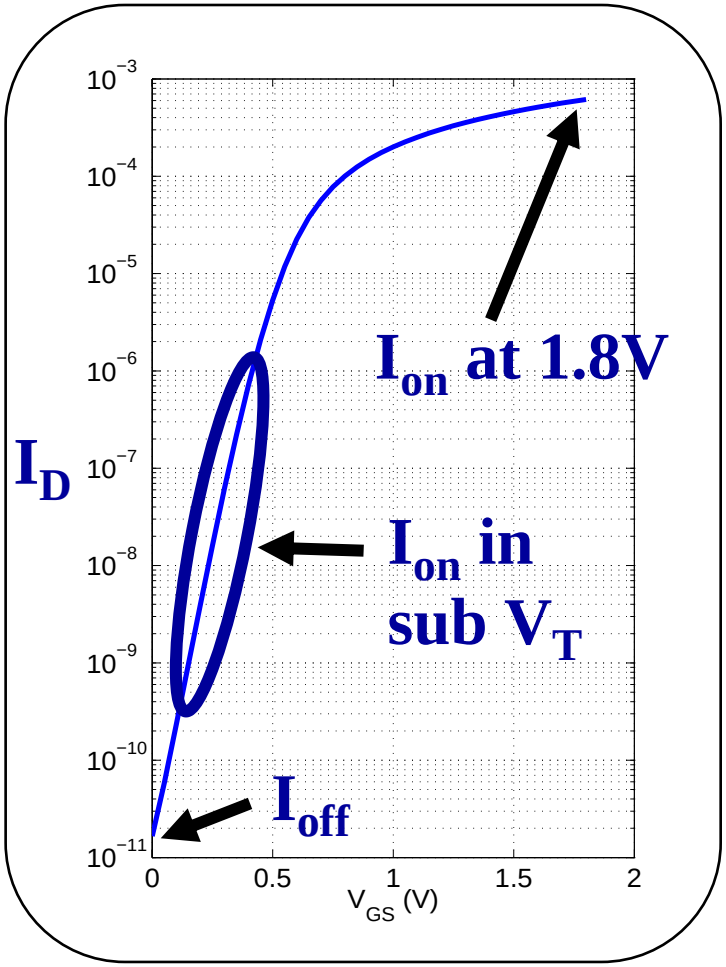
Process Balance: Outline

- **About Process Balance**
- Implications and Examples
- Modeling
- Conclusions

Sub-threshold Operation

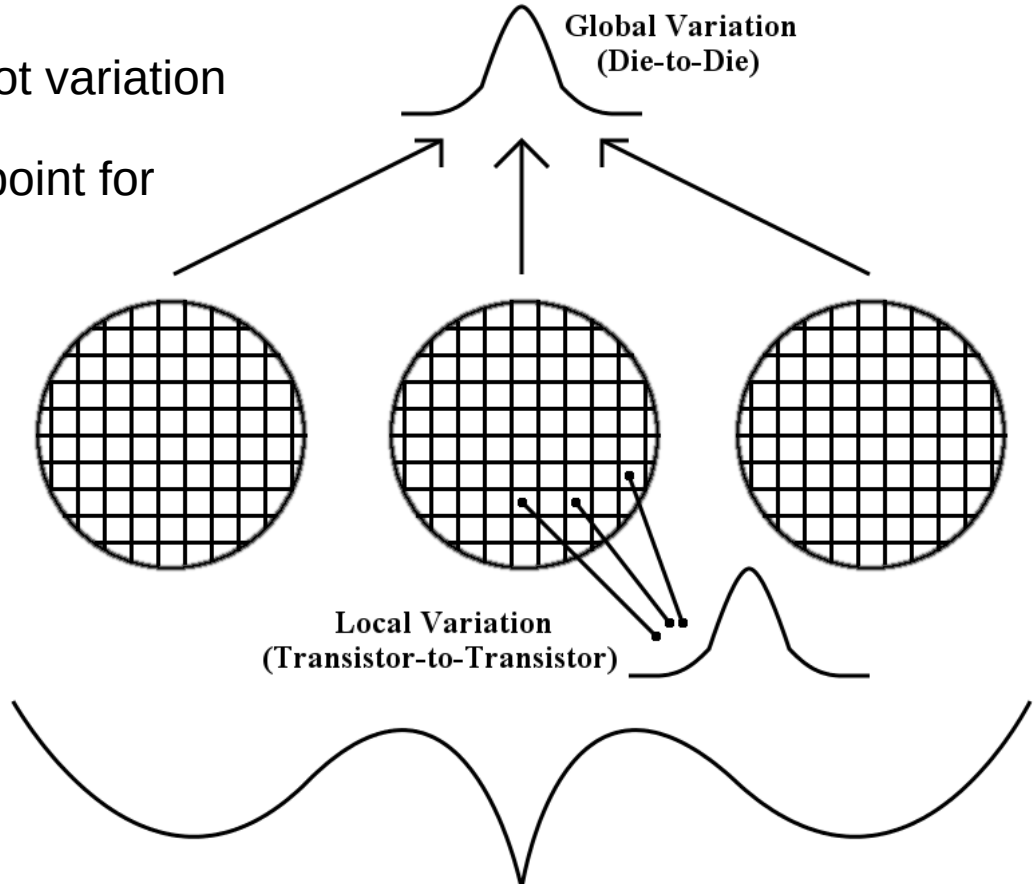


- $V_{DD}<V_T$
- Sub-threshold current for Ion and Ioff
- Well-suited for minimum energy or ultra-low power applications

Process Balance: What Is It?

Process Balance is not variation

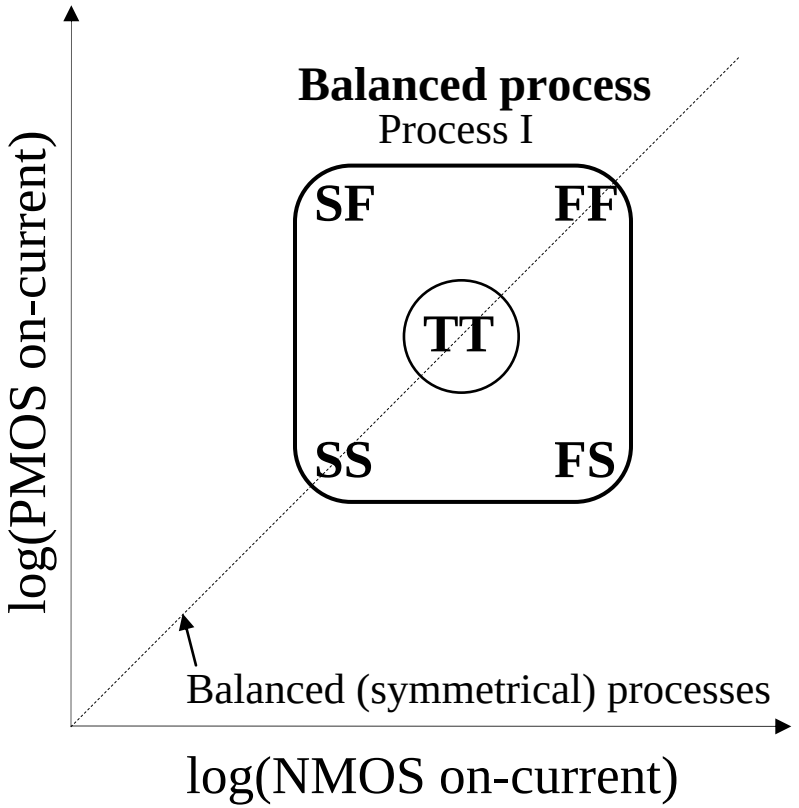
It sets the reference point for variation



Process Balance affects the reference point for all variations.
(e.g. the Typical NMOS, Typical PMOS (TT) process corner)

Process Balance: A Balanced Process

- Process Balance affects the Typical-Typical Point.
- Processes in strong inversion are all similar: NMOS ~2-3X stronger than PMOS
- Sub-threshold process balance can vary significantly from process to process
- Balanced Process most robust for sub-threshold (well-known)



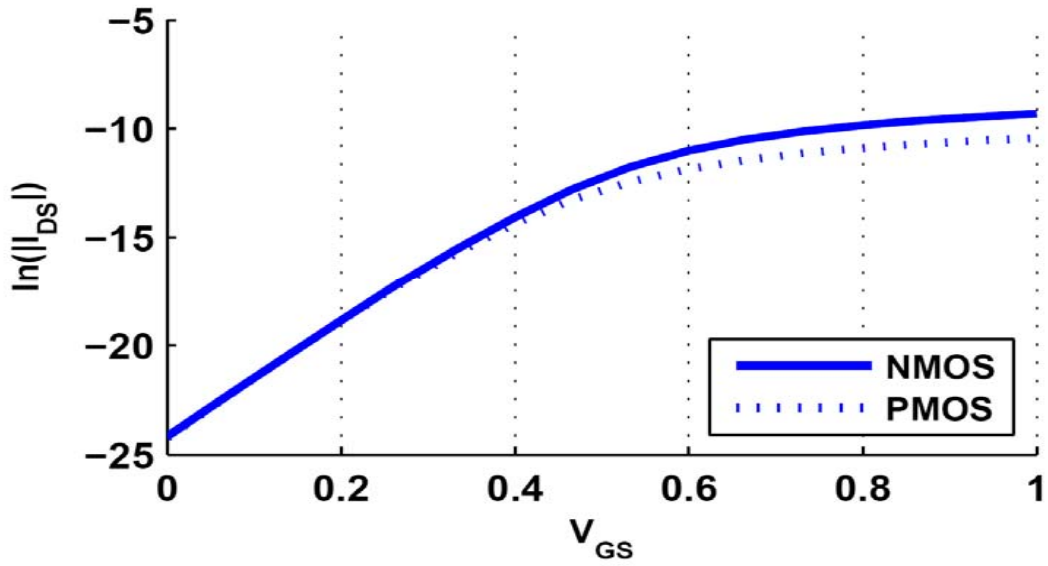
Process Balance: Formal Definition

- We define Process Balance as the ratio between the PMOS and NMOS currents in the sub-threshold region
- Process Balance Factor (PBF) = I_P / I_N
- Ideally, this ratio should be equal to 1 for a “balanced” process.

Example Balanced Process

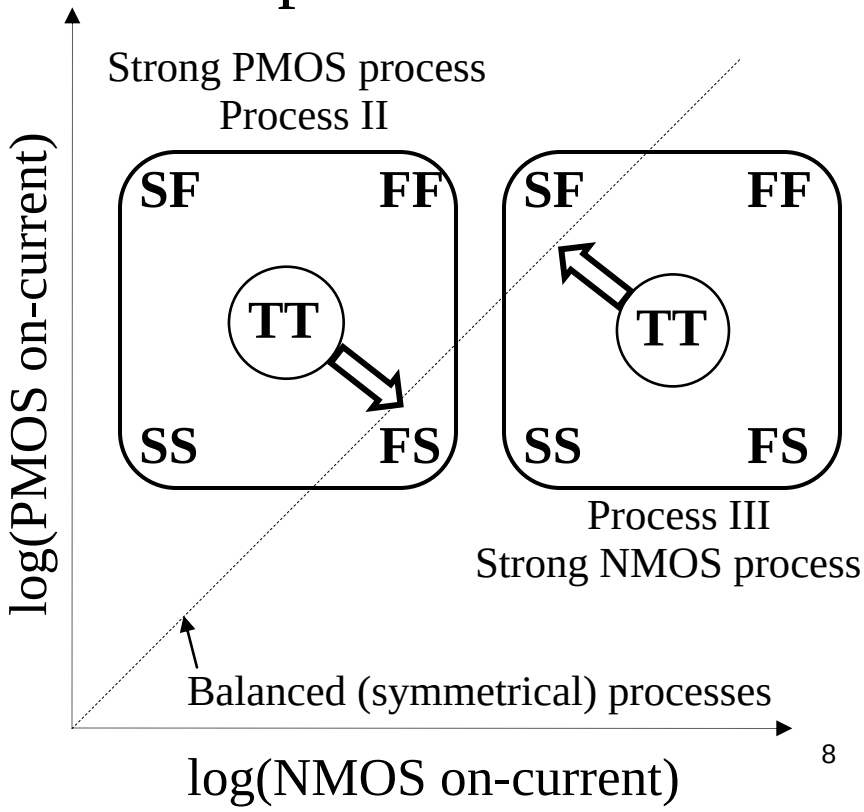
- $\ln(PBF) = \ln(I_P) - \ln(I_N)$
- $\ln(PBF) = \ln(I_{P\text{-}OFF}) - \ln(I_{N\text{-}OFF})$

PBF=1 (Balanced Process)



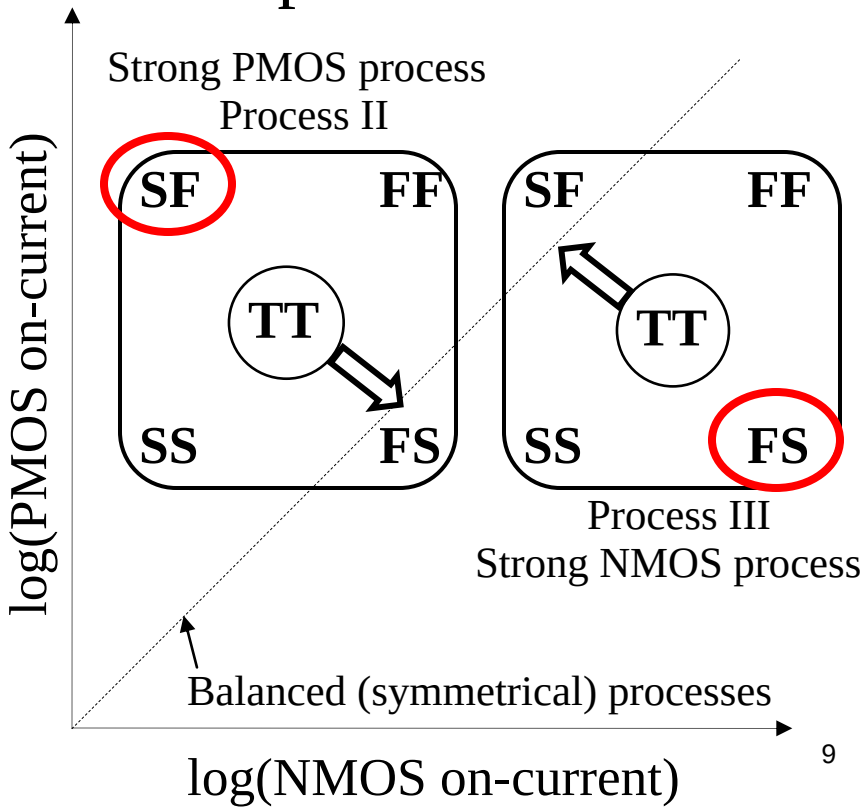
Process Balance: Imbalanced Processes

- Process Balance affects the Typical-Typical Point.
- Global variations have different impact for different process balance.



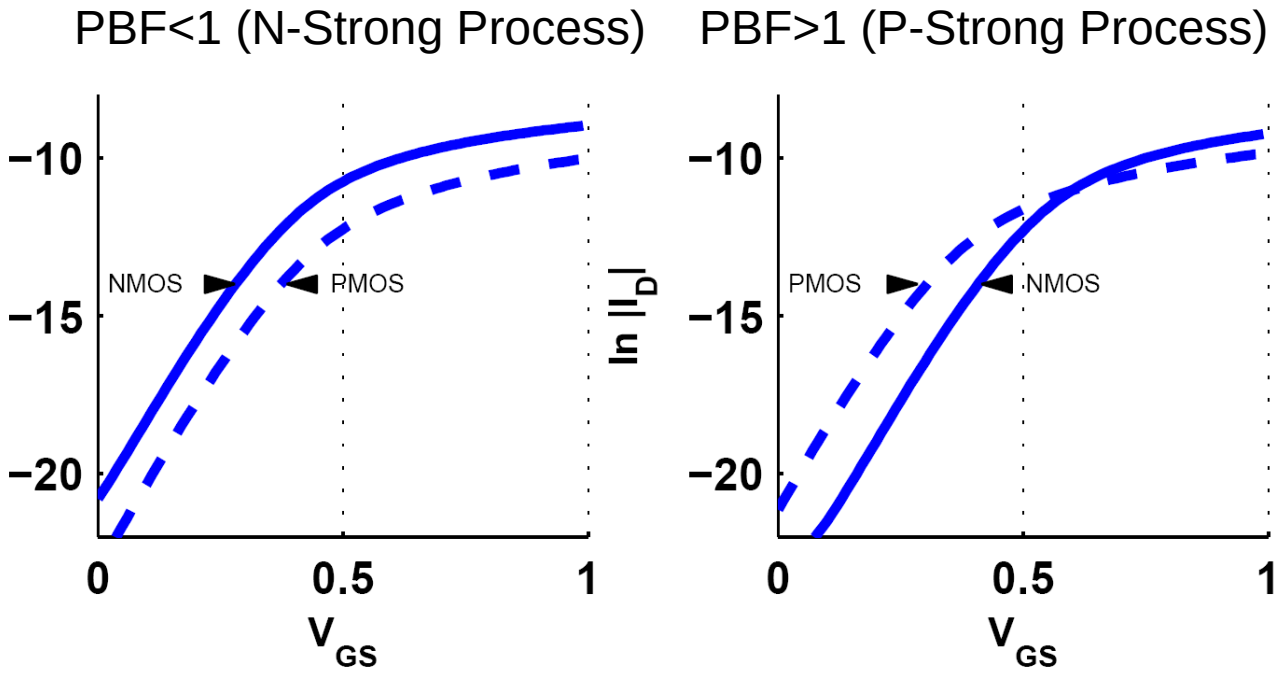
Process Balance: Imbalanced Processes

- Process Balance affects the Typical-Typical Point.
- Global variations have different impact for different process balance.
- **Worst Case Corner**
- **Different processes show different trends!**
- **Processes Balance has little correlation to the feature-size / vendor!**



Process Balance Factor: Example

- Fictitious processes are generated from the PTM (Predictive Technology Model) library by changing V_T for the PMOS and NMOS transistors.
- These examples correspond closely with real commercial processes

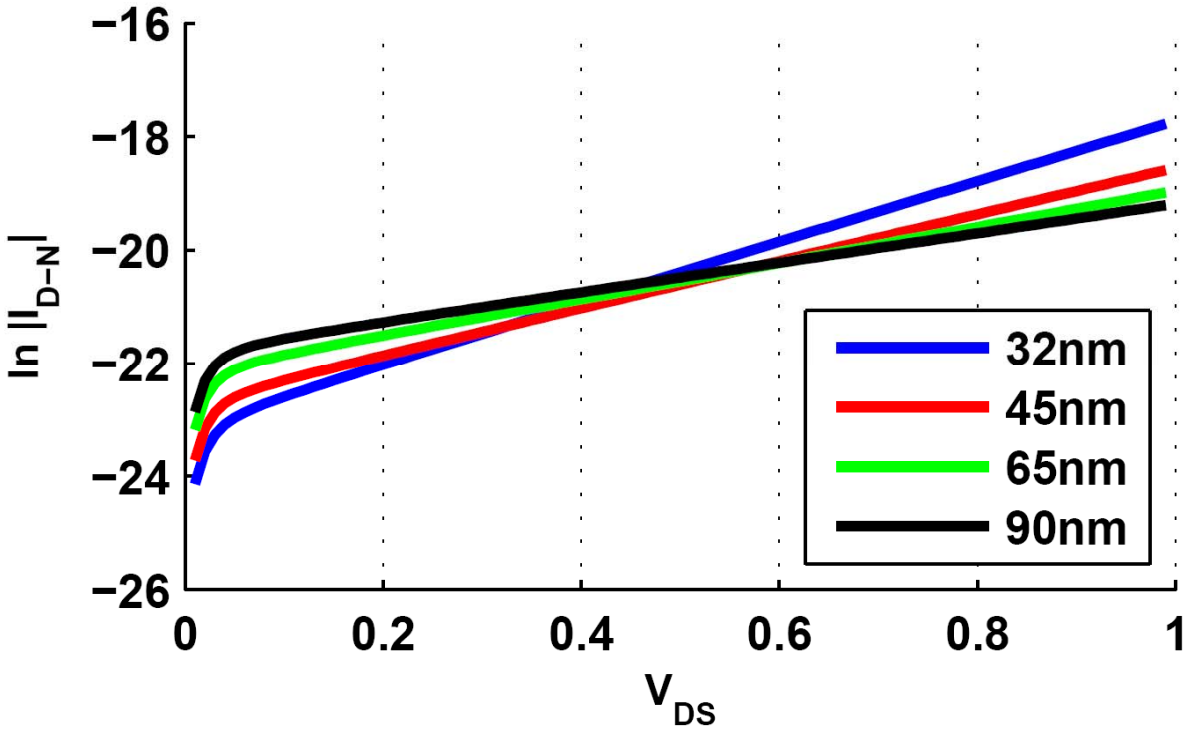


Process Imbalance: Where does it come from?

- In strong-inversion, mobility difference sets N/P current ratio to be approximately two.
- In sub-threshold, other effects dominate: Threshold voltage (V_T), sub-threshold slope, DIBL, etc. (terms in the exponent)
- V_T is the most important factor that affects process balance at sub-threshold voltages!!

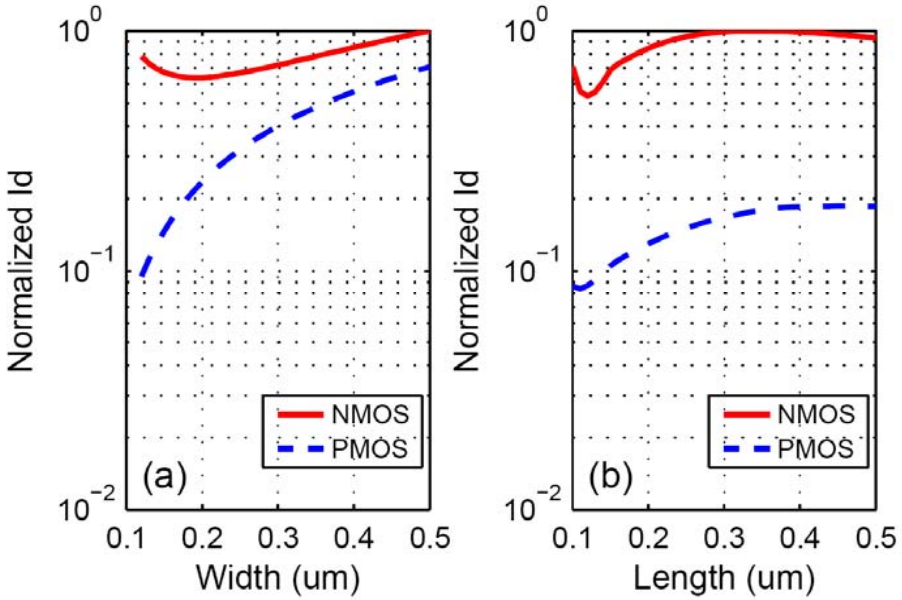
Process Imbalance: Where does it come from?

- Drain-Induced Barrier Lowering (DIBL) can cause the PBF to change with VDD



Process Imbalance: Where does it come from?

- Sizing
  - Non-minimum sized devices may have a different I_P/I_N ratio!
  - Small-channel effects: $V_T = f(W,L)$
- Temperature
  - May change the relative strengths of PMOS and NMOS devices. (small effect)



Analyzing Sub-threshold Circuits

- Rule of thumb: Check to see if a circuit change makes the process more or less balanced to analyze robustness

Process Balance: Outline

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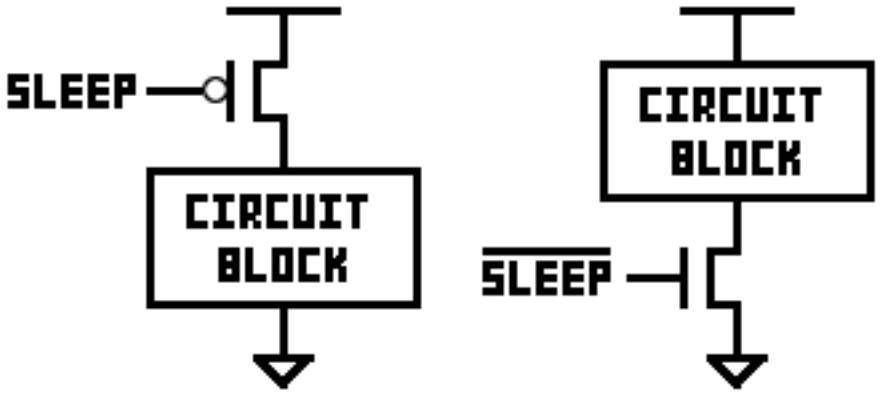
Reporting and Comparing Sub-V_T Circuits

- Process Balance impacts circuit choices
- Processes with different balance points most likely require different circuits
- **Main Point:** Generalizations for Sub-V_T circuits only apply to other processes with similar Process Balance Factors (PBFs).

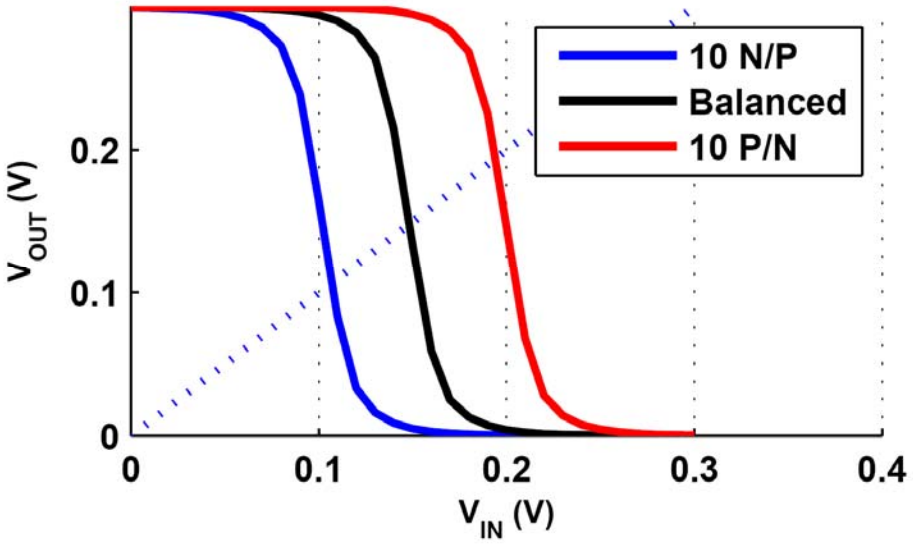
Implications on Leakage Control

- Process Balance has an effect on Leakage Control: On/off current ratio differs for P and N
- Power gating: gate the off-current using a PMOS device for a N-strong process, and with a NMOS device for a P-Strong Process.



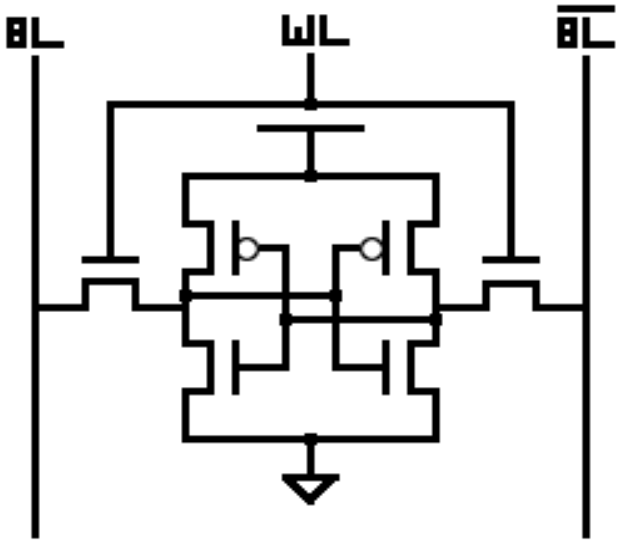
Implications for Combinational Logic in Sub-Threshold

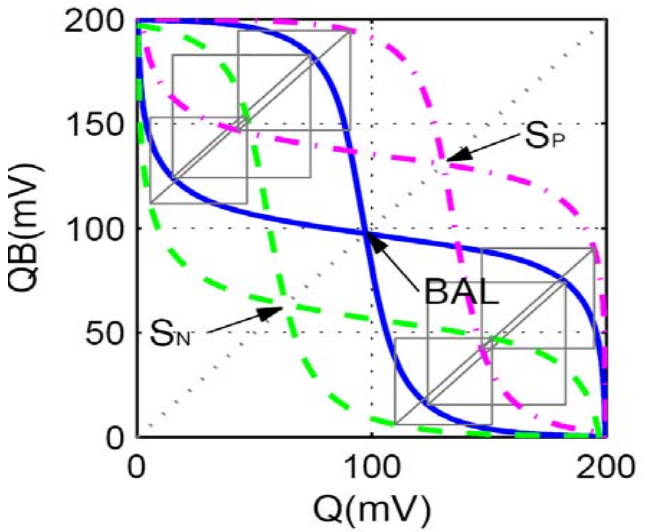
- Process Imbalance can have a large effect on noise margins.
- An order of magnitude difference in the PBF can cause a 30% shift in the switching threshold, V_M, of an inverter.
- Note that this is at the TYPICAL point; variations will make the switching worse!



Implications for SRAM Stability in Sub-Threshold

- Process Imbalance can affect SRAM stability at sub-threshold voltages.
- P-Strong moves TT trip-point above VDD/2
- N-strong moves TT trip-point below VDD/2

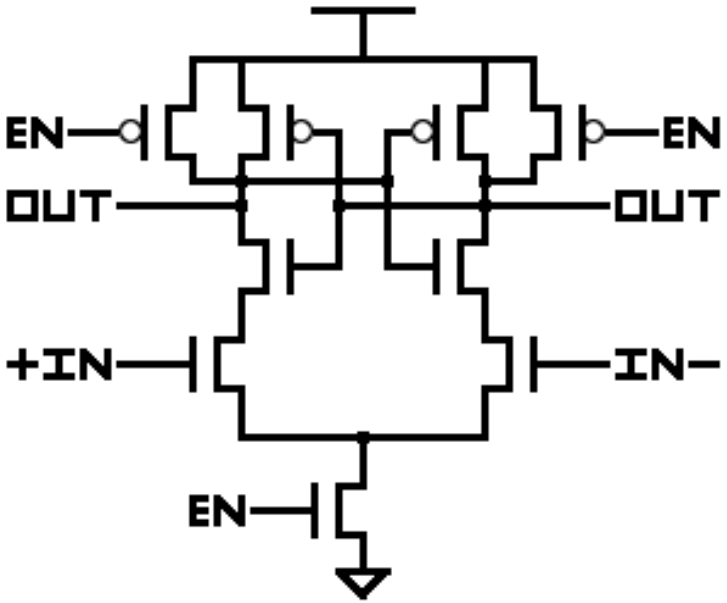




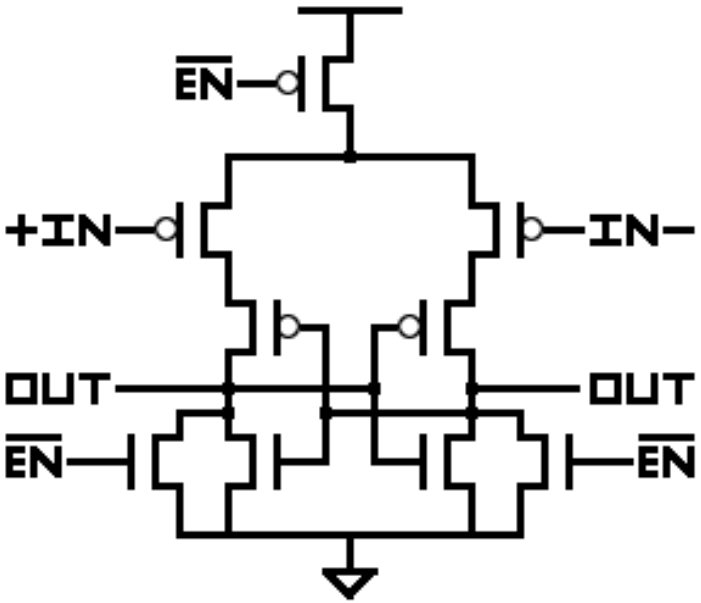
Implications for Sensitive Circuits in Sub-Threshold

- e.g. Process Imbalance can greatly effect resolution speed and even functionality of a sense amplifier in Sub-V_T.

N-Input SA

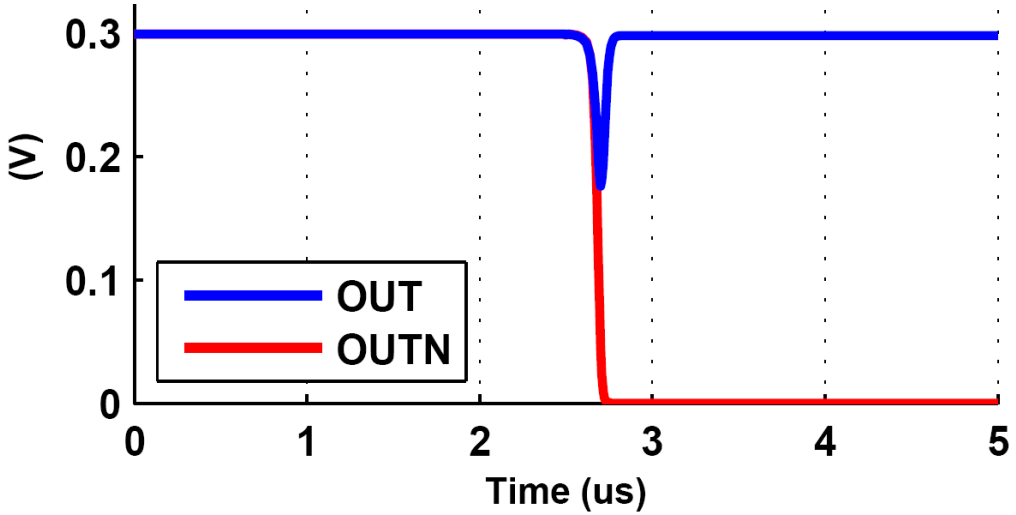


P-Input SA

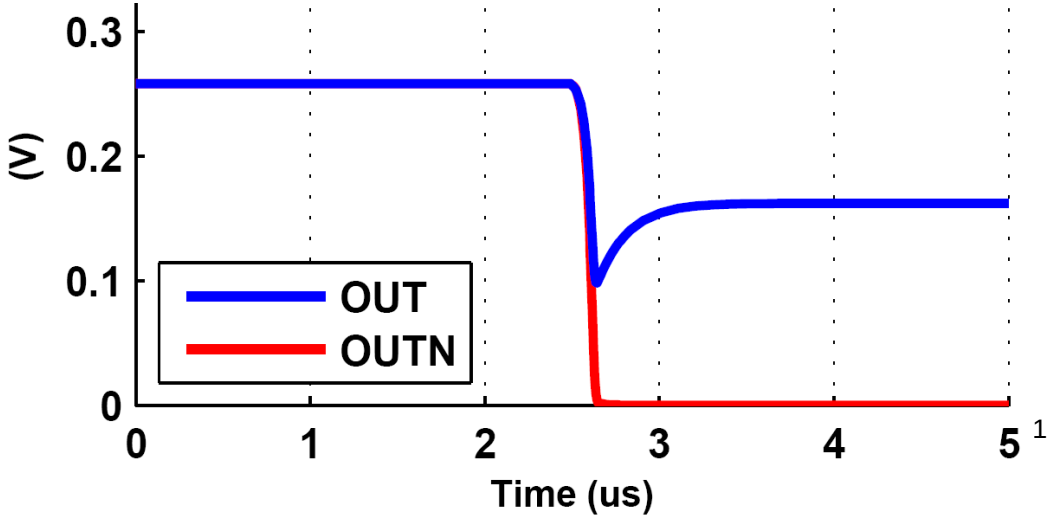


Implications for Sensitive Circuits in Sub-Threshold

- N-Input SA, V_{DD} =0.3V, N-Strong Process, TT Corner,



- N-Input SA, V_{DD} =0.3V, N-Strong Process, FS Corner



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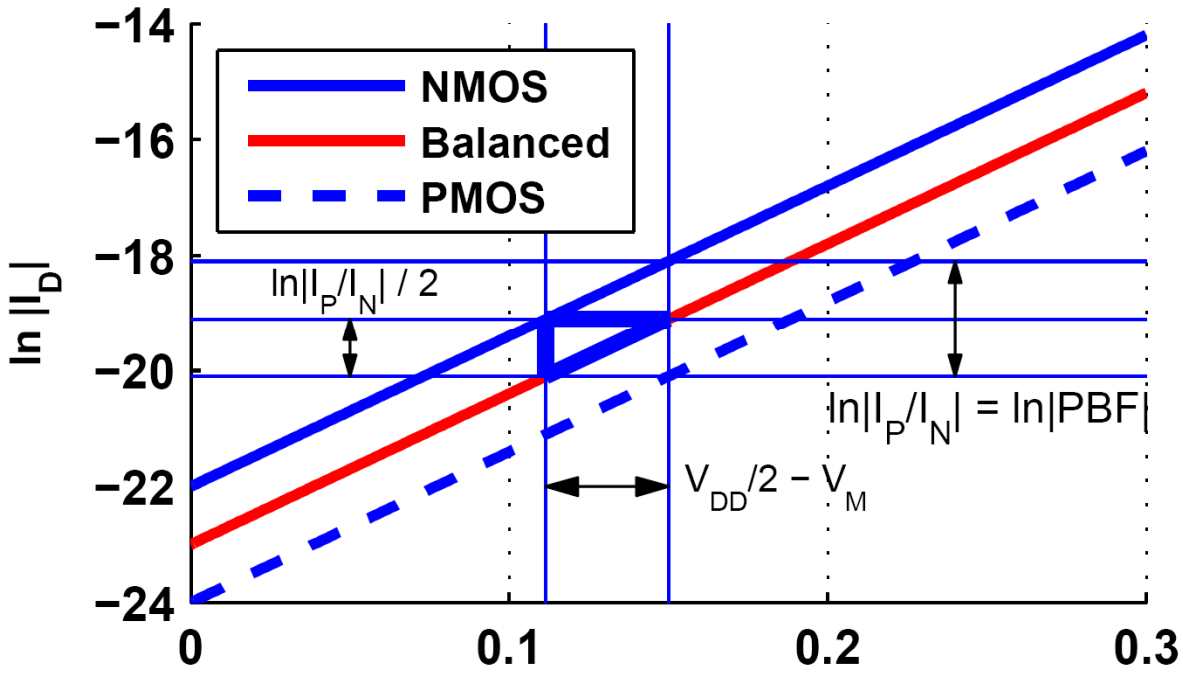
Modeling Process Balance

- As shown, Process Imbalance effects Noise Margins most seriously
- Use an inverter to model this effect

Modeling Effects of Process Balance

- Model inverter V_M using by using Process Balance concept:
- If N-Strong, $V_M < V_{DD}/2$
- If P-Strong, $V_M > V_{DD}/2$
- V_M can be found with simple geometry; $V_M = VDD/2 + S*\log(PBF)/2$



Modeling Effects of Process Balance

- To contrast, VM can be found analytically:

$$V_M = \frac{V_{DD} n_n (1+\eta_p)}{n_n(1+\eta_p)+n_p(1+\eta_n)} + \frac{n_p V_{Tn} - n_n V_{Tp}}{n_n(1+\eta_p)+n_p(1+\eta_n)} + \frac{n_n n_p V_{th} \ln\left(\frac{(W/L)_p I_{op}}{(W/L)_n I_{on}}\right)}{n_n(1+\eta_p)+n_p(1+\eta_n)} + \frac{n_n n_p V_{th} \ln\left(\frac{1-\exp((-V_{DD}+V_M)/V_{th})}{1-\exp(-V_M/V_{th})}\right)}{n_n(1+\eta_p)+n_p(1+\eta_n)}$$

n_x=Sub-Threshold slope factor, η_x=DIBL Coefficient, V_{th} = kT/q

- By assuming equality between NMOS and PMOS devices (other than in V_T) and by ignoring the last term, one can show that this equation equals the one on the previous slide.

Modeling Effects of Process Balance

- Assume symmetry in N and P except for V_T and ignore DIBL (η_x=0):

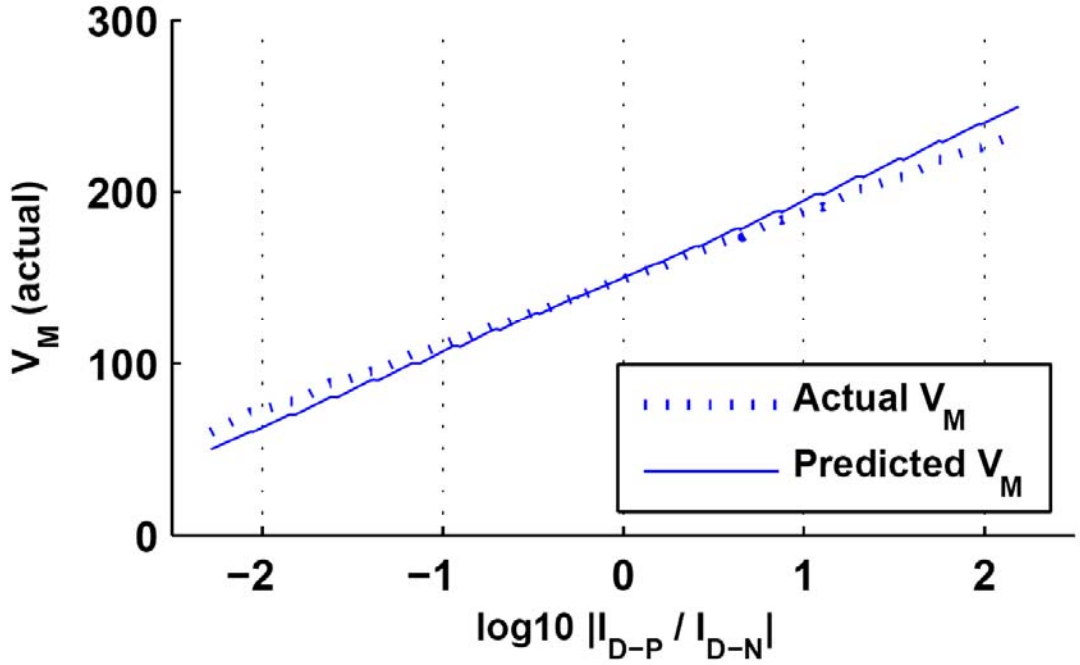
$$V_M = \frac{V_{DD}}{2} + \frac{V_{Tn} - V_{Tp}}{2} + \frac{nV_{th} \ln\left(\frac{1 - \exp\left((-V_{DD} + V_M)/V_{th}\right)}{1 - \exp\left(-V_M/V_{th}\right)}\right)}{2}$$

- Rightmost term models saturation near rails due to current roll-off. Ignore it if not near the rails:

$$V_M = \frac{V_{DD}}{2} + \frac{V_{Tn} - V_{Tp}}{2} = \frac{V_{DD}}{2} + \frac{S \log\left(PBF\right)}{2}$$

Modeling Effects of Process Balance

- Mean Percent Error ~ 3.2%
- Max Percent Error ~ 12% at PBF ~ 1/200
- Accurate model across 5 orders of magnitude.



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Conclusions

- Process Balance strongly affects most aspects of sub-threshold integrated circuit design
- Designs may not be portable between processes with widely different PBF (Process Balance Factor, the P/N current ratio).
- It is possible to use simple models to analyze the effects of process imbalance.

Thank you

- Any questions?