

A Battery-less 507nW SoC with Integrated Platform Power Manager and SiP Interfaces

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Abstract – A 507nW self-powered SoC is demonstrated for ultra-low power (ULP) internet-of-things (IoT) applications. The SoC includes ULP system-in-package (SiP) interfaces that enable its harmonious integration with a radio transmitter (TX) and a non-volatile memory (NVM). The energy harvesting platform power manager (EH-PPM) powers the SoC as well as off-chip components and is optimized for low quiescent power. It supplies the SoC with 0.5V, 1.0V, and 1.8V and can also power ULP sensors and the SiP components while running an example shipping-integrity tracking algorithm. A power monitor (PM) cold-boots the SoC from NVM and adapts the system's power consumption. The tight integration between the SoC's blocks enables sub- μ W operation.

As the semiconductor industry races towards 1 trillion IoT devices, there is an urgent need for ULP systems ($<10\mu$ W) capable of sensing, processing, and transmitting data. A number of promising low power [1-2] and self-powered [3-6] systems have been proposed. However, battery-powered systems [1-3] are not sustainable in an IoT vision due to the limited number of battery recharge cycles and the huge scale and cost of battery replacement. Self-powered processors such as [4] must be integrated into larger systems with more memory and a communication interface to support diverse IoT applications. SoCs such as [5-6] address this issue but cannot recover their program data after power loss.

We present a battery-less system-on-chip (SoC) designed as part of a SiP with a 1Mb/s FSK TX and NVM (Fig. 1) to leverage the advantages of different technologies, increase flexibility, and reduce cost and form factor. An EH-PPM harvests energy into a super-capacitor and regulates it to supply the SoC and off-chip components while drawing low (~ 400 nA) quiescent current. Flexible custom interfaces allow the SoC to communicate efficiently with SiP components and reduce their power. The PM controls the system power to keep it within the harvester's power budget. The core blocks are co-designed to achieve sub- μ W power consumption.

Fig. 2 shows a block diagram of the SoC, its main building blocks, and its interfaces to the TX and NVM. The SoC consists of the EH-PPM, the PM with a cold-boot management system (CBMS), an analog (ECG AFE with 12-bit ADC) and two digital (SPI, GPIO) sensing interfaces, a custom low power controller (LPC), a suite of hardware accelerators, and an ULP 32KHz oscillator.

The EH-PPM (Fig. 3) powers the SiP chips while drawing very low operating current. It harvests from either photovoltaic (PV) cells or thermoelectric generators (TEG) using either a single-inductor boost converter with maximum power point tracking (MPPT) control [8] or a fully integrated (no external passives) voltage doubling switched-cap harvester. In our integrated system, the harvested energy is stored on a 10mF super-capacitor. The EH-PPM also includes three fully integrated regulators that deliver a 0.5V subthreshold rail for the SoC core system, a 1V rail for the SoC pads and the in-package sub-systems, and a 1.8V rail to power sensing interfaces and off-chip sensors. The regulators are specifically

designed to handle sub- μ W loads and use load-dependent pulse frequency modulated control and nW-power error amplifiers, comparators, and reference generators to reduce their I_{DDQ} . A power on circuit ensures a sequenced turn-on of the different regulators before enabling the system. Once the power rails are established, the PM handles the startup of the system, keeps track of the available energy, controls off-chip components and adjusts the power consumption of the system.

Integrating and managing NVM within a battery-less system budget is challenging because of the inherent high power nature of most NVM technologies. Thus, an ULP in-package cold-boot bus (CBB) interfaces between the SoC and NVM. The CBB reduces the NVM's on time and the SoC boot-up time through bus parallelization and avoids the overhead of generating a high frequency serial interface. Its reduced swing operation cuts down the communication cost, optimizing the NVM's integration within the SiP. To enable full recovery after a power-on-reset (POR), the PM instructs the CBMS to retrieve data from NVM when the available energy exceeds a boot-up threshold. The CBMS is also responsible for programming the SRAM instruction memory during boot-up, and backing up critical data before power loss. Fig. 4 shows the boot-up and back-up sequences.

The SRAM and LPC are tightly coupled to create various power saving modes. The SRAM is designed for battery-less systems with its high- V_T 8T bit-cell and myriad power saving techniques [9]. The LPC takes full advantage of these SRAM features resulting in significant (up to 66%) measured power savings (Fig. 5). The LPC instruction set (with Python based assembler) and integrated accelerators target IoT applications and thus allow users to develop compact programs to reduce power consumption without sacrificing functionality.

The SoC core architecture is carefully designed to enable sub- μ W operation. Each accelerator is tightly integrated with the block using it to eliminate the need for direct memory access. For example, the compression accelerator (lossless entropy compression algorithm GAS-LEC) is integrated in the radio interface (RI) to lower communication costs. Similarly, the heart rate and afib (RR-AFIB) monitor is integrated with the ECG front end (designed to operate in sub-threshold for low power). The SoC also includes two general purpose timers, an FIR filter, and a MAC unit for data processing.

We demonstrated the SoC with a shipping-integrity tracking application that uses the SPI, GPIO, compression, and radio interface. A flowchart of the program is presented in Fig 6. Fig 7 shows the power up sequence and the power distribution during different operating conditions. Data transmission from the TX, coupled to the SoC, is shown in Fig 8. Fig 9 presents a comparison to state-of-the-art μ W-level SoCs.

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References

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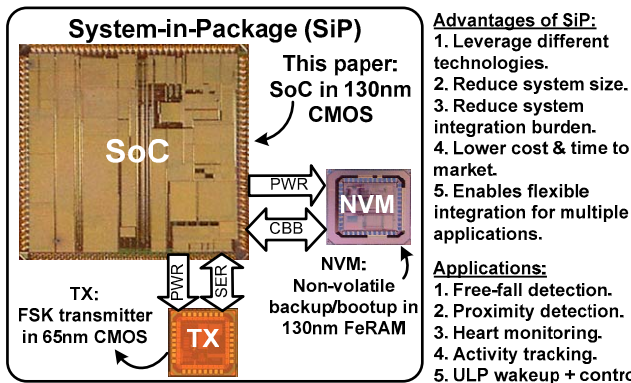


Fig. 1. The proposed SoC fabricated in 130nm CMOS with flexible interfaces to NVM and TX to enable harmonious integration in a SiP.

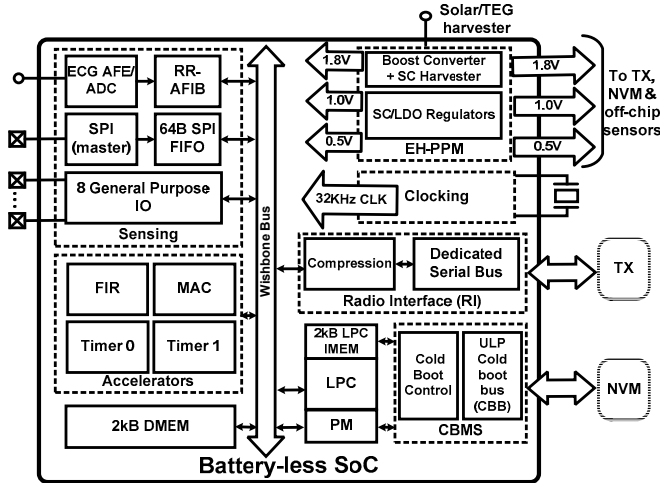


Fig. 2. Block diagram of SoC showing harvesting system, sensing modalities, accelerators, cold-boot management, and radio interface.

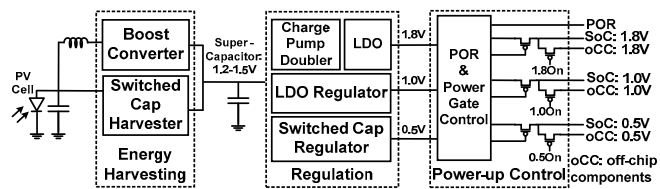


Fig. 3. EH-PPM sub-system with a voltage doubler for PV harvesting, 3 regulators, and a power-up controller. The user can program 1.80n, 1.00n and 0.50n to supply off-chip components if needed.

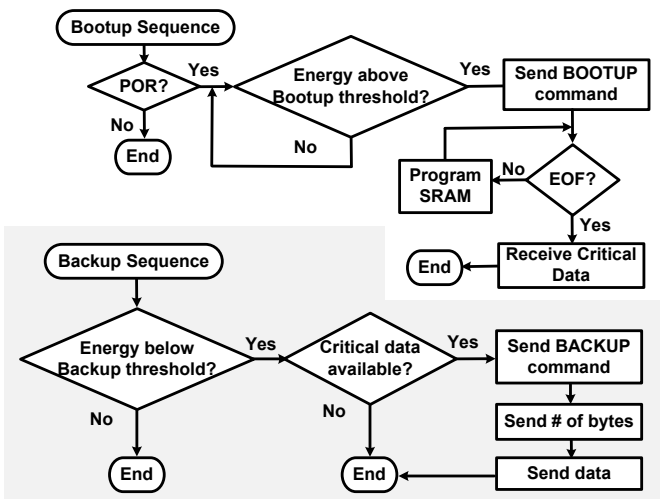


Fig. 4. The boot-up sequence retrieves data from NVM. The back-up sequence stores system critical data in NVM before power loss.

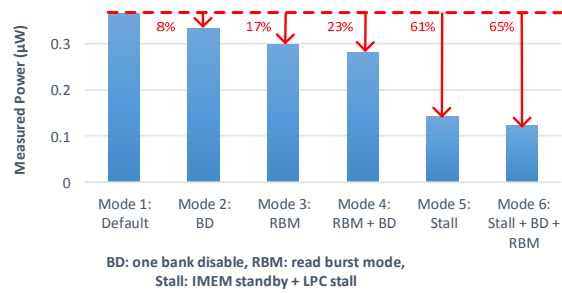


Fig. 5. The SRAM power modes reduce the measured power consumption of the Control block (LPC+IMEM+PM+CBMS+RI).

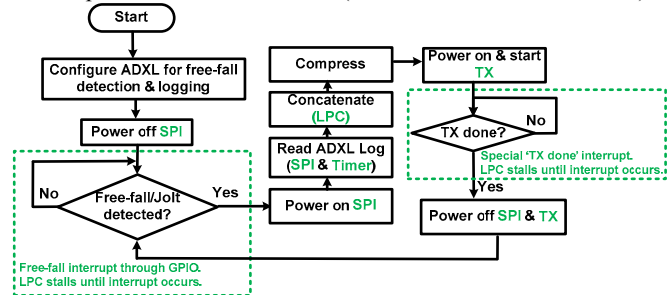


Fig. 6. Flowchart showing the shipping-integrity tracking algorithm implemented using the ADXL362Z free-fall feature and TX chip.

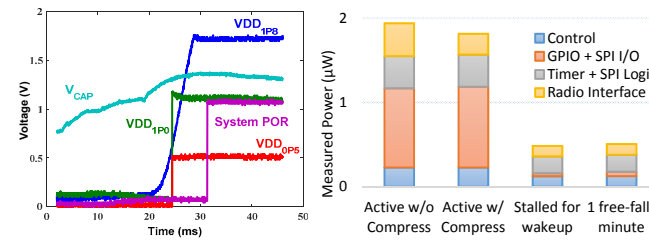


Fig. 7. (Left) The measured power up sequence before the system POR is asserted. (Right) Distribution of measured power with and without compression and assuming 1 free-fall/minute (pessimistic).

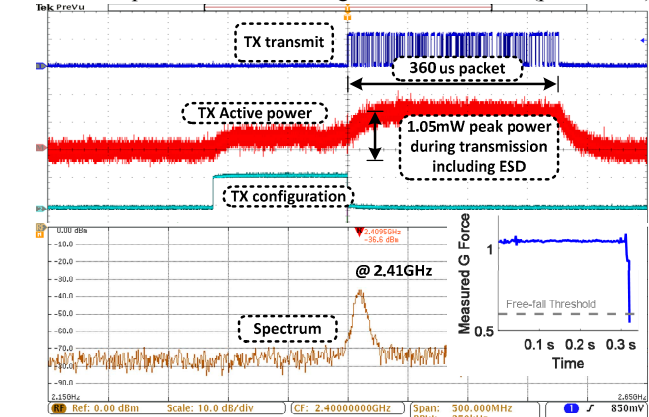


Fig. 8. Meas'd radio transmission through TX chip. Inset: Meas'd free-fall data for shipping-integrity tracking transmitted from SoC.

	This work	[2]	[3]	[4]	[5]
Battery-less	Yes	No	No	Yes	Yes
Harvests power	Yes	No	Yes	Yes	Yes
Fully integrated EH-PPM	Yes	No	No	No	No
Powers off-chip Sensors	Yes	No	No	No	No
Regulated voltages	1.8V, 1.0V, 0.5V	0.25V-1.2V	-	unregulated	1.2V, 0.5V, variable
Interface to NVM	Yes	No	No	No	No
On-chip SRAM	4KB	24KB	3.7KB	256B	12KB
Accelerators	5	2	3	-	7
Sensing interfaces	3	2	1	-	2
Total Power	507nW	850nW	45nW	295 pW	2.3µW
Components Included in Total Power	MCU + SPI + IO + Timer + GPIO + RI	MCU	AFE + DSP	MCU	MCU + IO + SPI +

Fig. 9. Comparison to state-of-the-art SoCs. MCU: main controller + instruction memory.