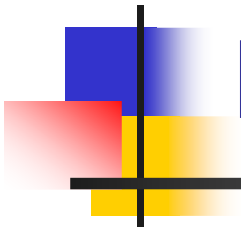
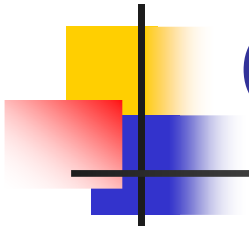


Asymmetric 6T SRAM with Two-phase Write and Split Bitline Differential Sensing

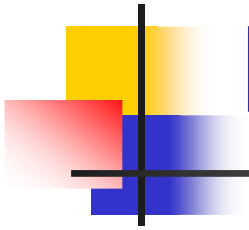
Satyanand Nalam and Benton H. Calhoun
University of Virginia, Charlottesville, VA

Vikas Chandra, Cezary Pietrzyk, and Robert C. Aitken
ARM, San Jose, CA



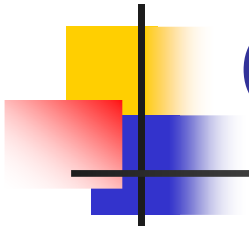
Overview

- Motivation
- Asymmetric 6T bitcell
  - Basic Idea
  - Two-phase write
  - Comparison with 6T
- Split BL sensing
  - Basic Idea
  - Comparison with differential sensing
- Conclusions



Motivation

- Low voltage operation ⇒ Power ↓ *BUT* Read & Write NMs ↓
- Improve Read NM ⇒ Write NM worsens and vice-versa
- How to improve both at the same time?
  - Decouple read and write
  - Alternative cells – e.g. 8T



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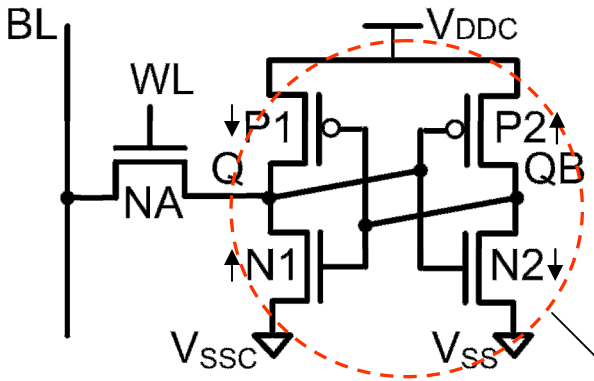
Basic Idea

Asymmetric 5T

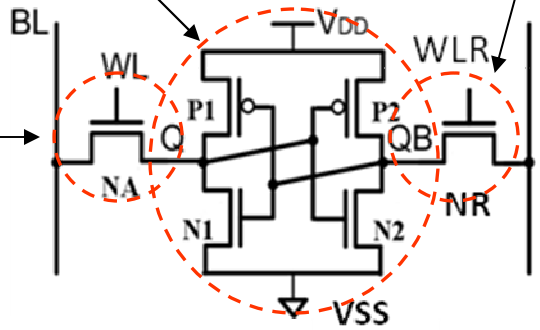


[Nalam, CICC '09]

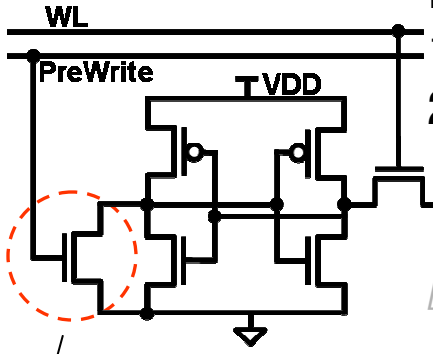
Problems?
1. Write
2. Single-ended Sensing

1. Asymmetric sizing

3. Large ⇒ Good WM, Less Rd & Write delay



5T with Reset



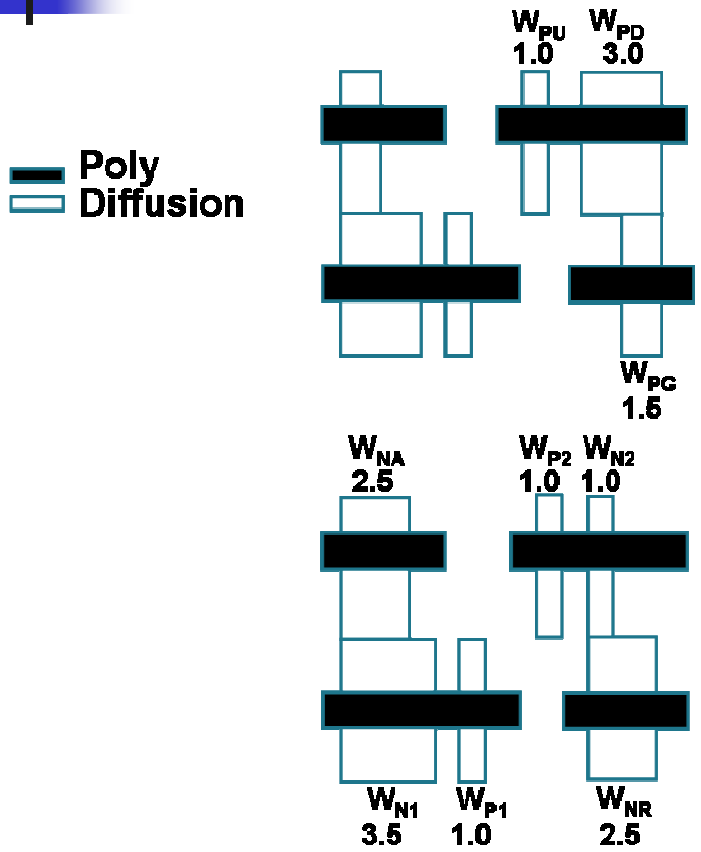
Problems?
1. No col-mux
2. Single-ended Sensing

[Dehaene, ESSCIRC '07]

2. Reset cell to '1'

Asymmetric 6T with dual WLs, iso-area

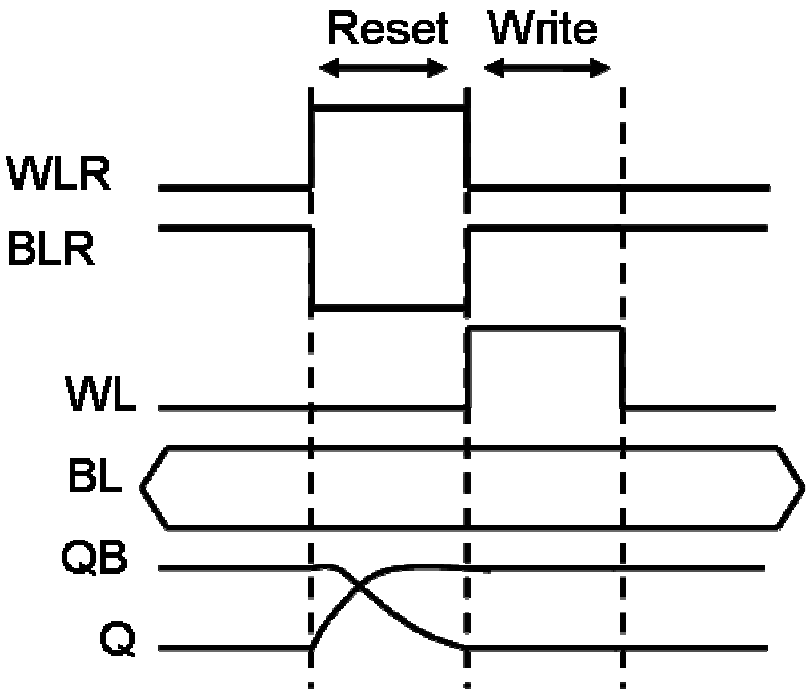
Sizing approach



W6T = 2*(max (WPD, WPG) + WPU)
= 8.0

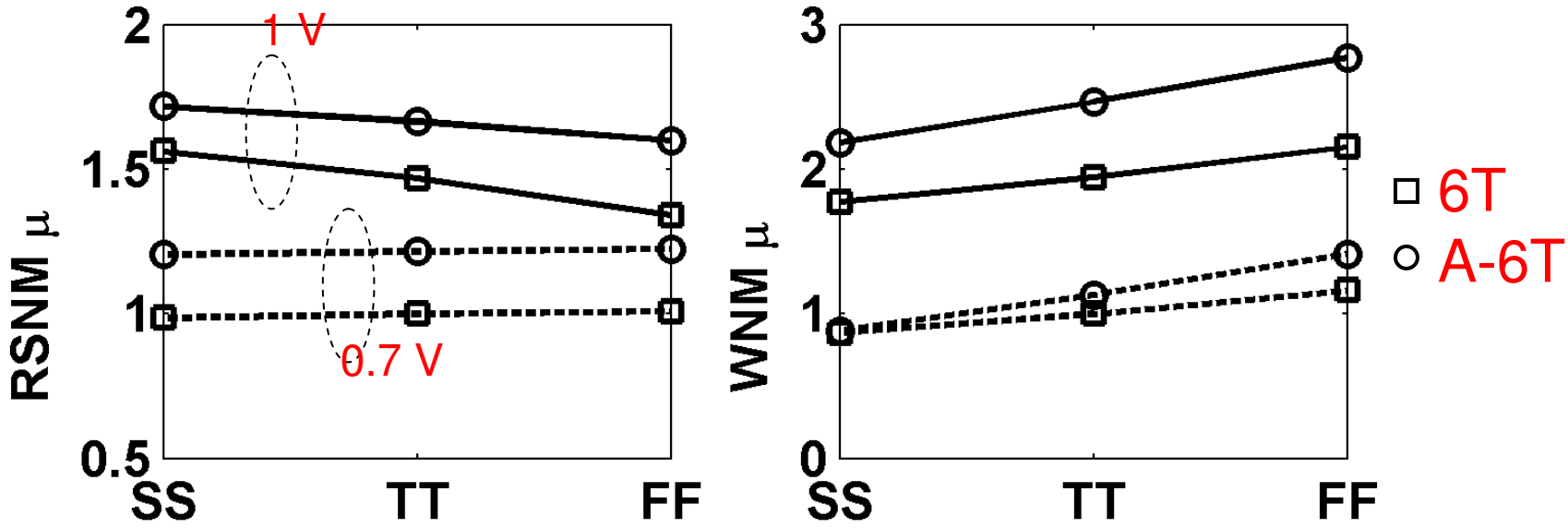
W6T = max (WN1, WNA) + WP1 + WP2 + max (WN2, WNR)
= 8.0

Write operation



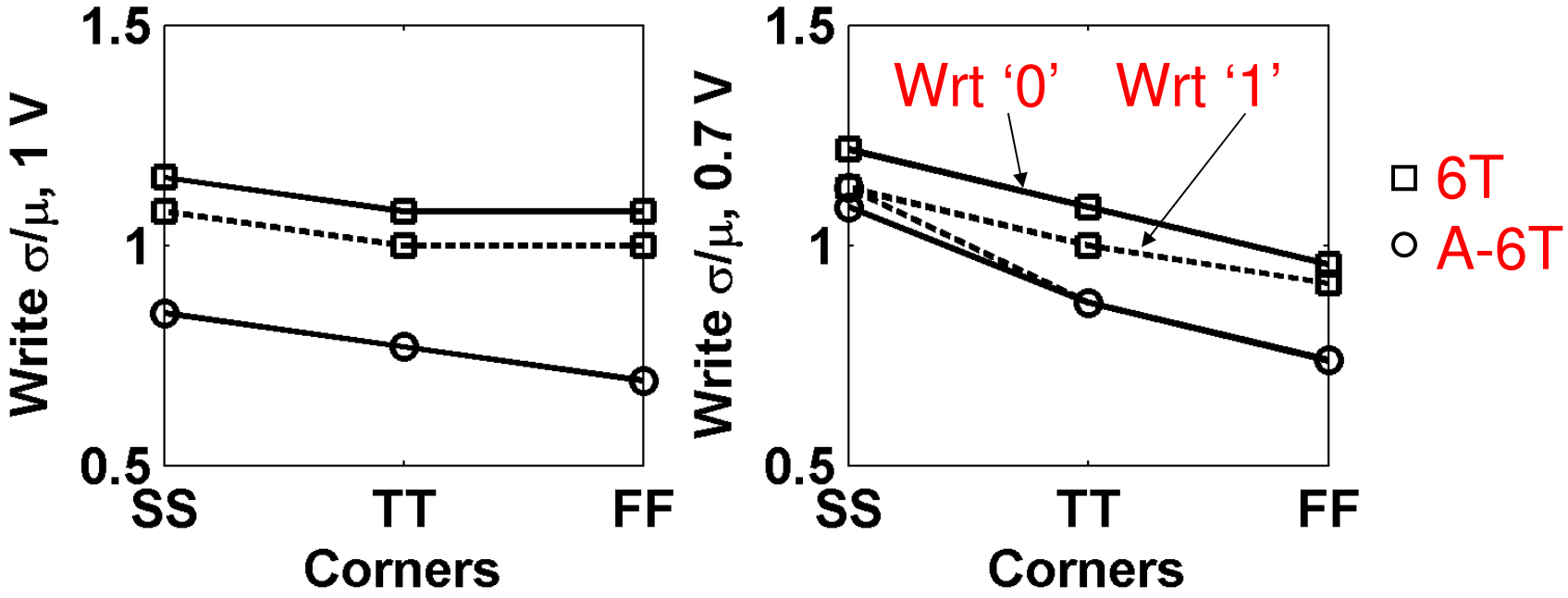
Two-step write –
1. Reset all selected cells to ‘1’
2. Write ‘0’ where needed

Comparison with 6T: Noise margins



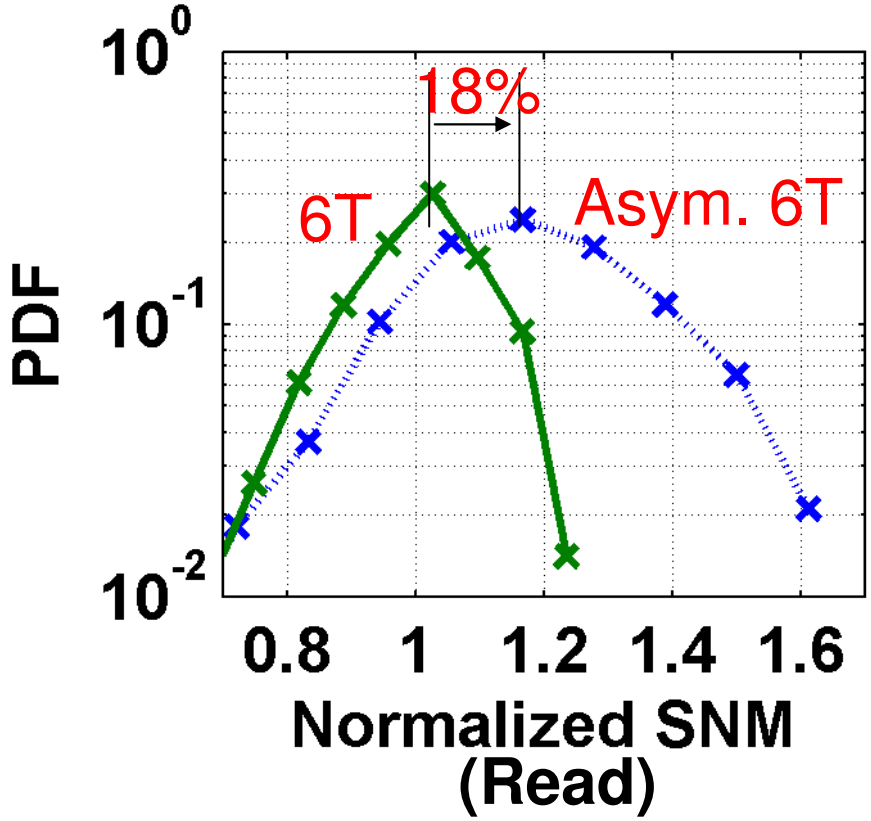
Mean NMs improve across corners and V_{DD}

Comparison with 6T: Noise margins



σ/μ of WNM for '0' and '1' both improve across corners and V_{DD}

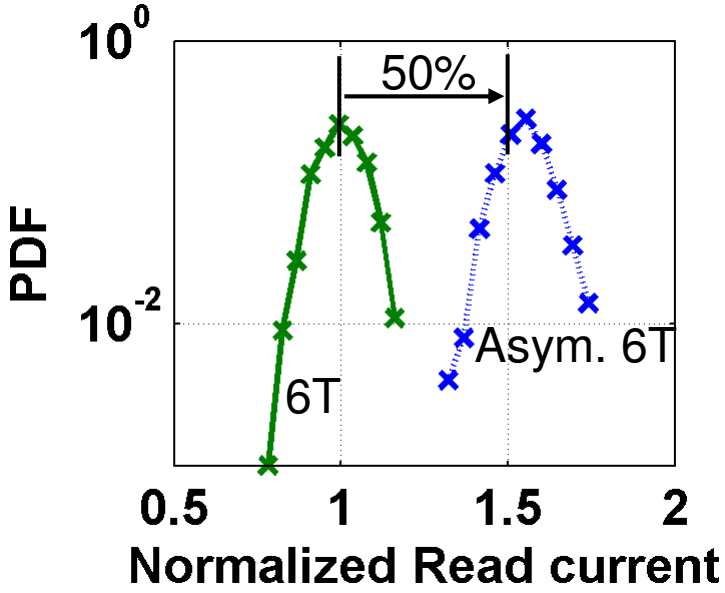
Comparison with 6T: Noise margins

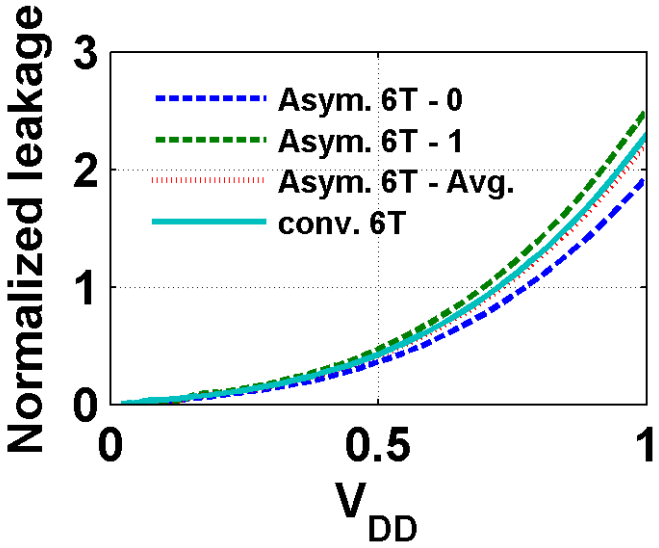


From simulation:

- Rd-V_{MIN} ↓ by 21.5%
- Wrt-V_{MIN} ↓ by 4%

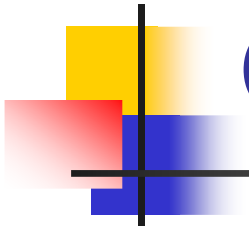
Comparison with 6T: Read current and cell leakage





Wider Pull-down increases I_{READ}

- Data-dependent leakage
- More '0's ⇒ less leakage



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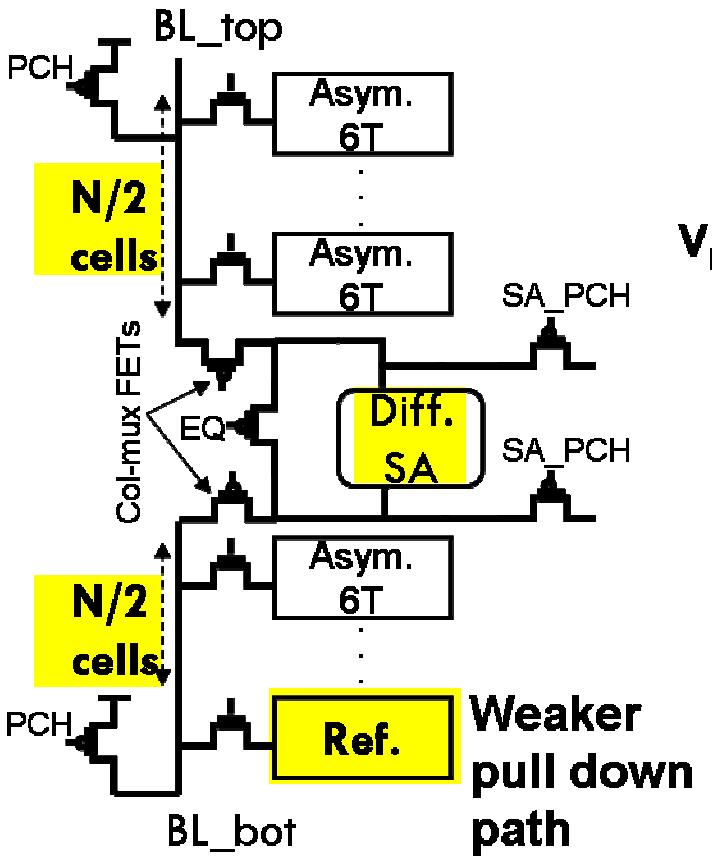
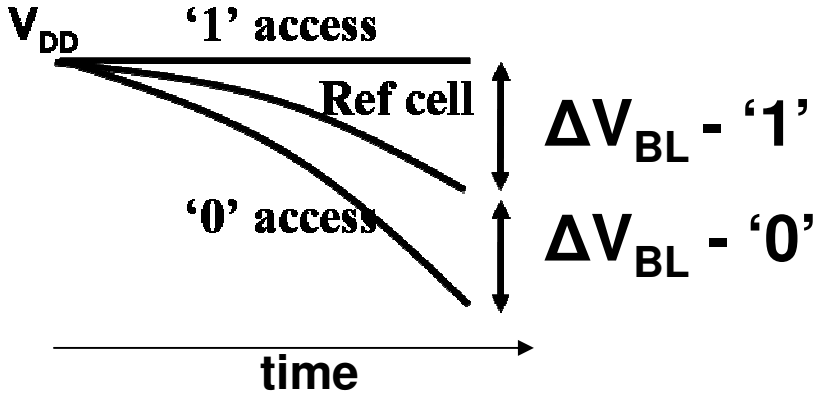
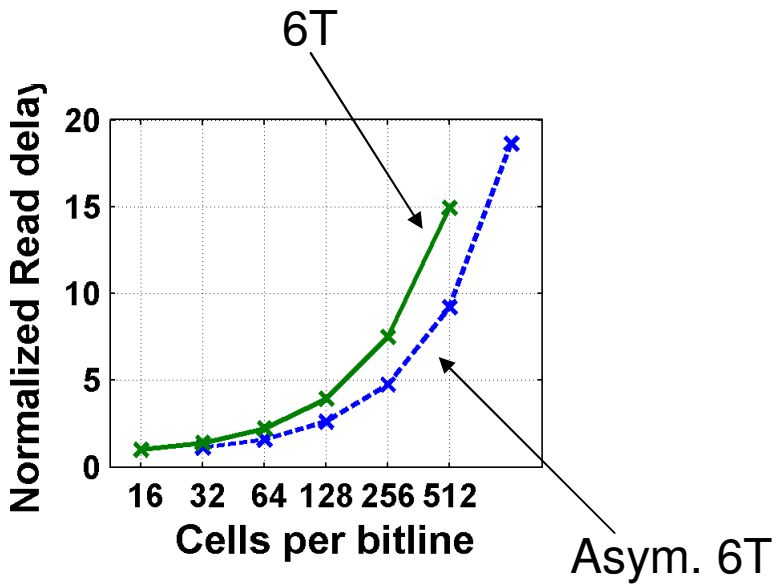
Sensing scheme



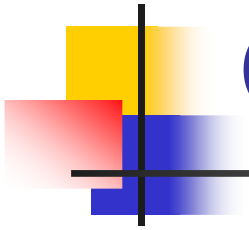


Comparison with differential sensing



Improved read performance -

- #cells/discharging BL halved
- Better I_{READ}



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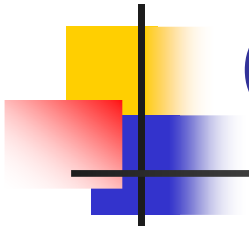

Conclusions

- Asymmetric 6T cell
  - Increased NMs, Lower V_{MIN}
  - Single-ended operation
- Single-ended/pseudo-differential sensing
  - Leverage improved I_{READ}
  - Extensible to any single-ended bitcell