Asymmetric 6T SRAM with Two-phase Write and Split Bitline Differential Sensing for Low Voltage Operation

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Abstract

This paper describes an asymmetric single-ended 6T SRAM bitcell that improves both Read Static Noise Margin (RSNM) and Write Noise Margin (WNM) for the same bitcell area as a conventional symmetric 6T. This improvement is achieved using a single V_{DD}, without employing assist techniques that require multiple voltages. The improvement in noise margins significantly improves the low-voltage robustness and consequently the minimum operating voltage of the SRAM (V_{MIN}). Single-ended write is accomplished in two phases using dual word-lines. Finally, we propose a differential sensing scheme using a weak reference cell to read the single-ended 6T. A combination of reduced bitline capacitance and increased drive current ensure read delay comparable to conventional differential sensing, for the same bitcell area.

1. Introduction

Increasing power consumption is a major problem in modern ICs. Low-voltage operation provides power-savings or longer battery life depending on the application. However, voltage scaling for conventional six transistor (6T) bitcells is difficult due to decreasing noise margins and increasing variation [1]. This is a consequence of the careful balance that needs to be struck between the conflicting requirements of read and write operations. Thus, reducing the lowest operating voltage, V_{MIN}, is a challenge. In this work, we propose a bitcell with improved robustness compared to the conventional 6T bitcell that can enable lower-power operation by lowering V_{MIN}.

To improve bitcell robustness, several alternative bitcell structures have been proposed. The 8-transistor (8T) bitcell [2] and the 7-transistor (7T) bitcell [3] decouple the read and write operations. This allows Read Static Noise Margin (RSNM) and Write Noise Margin (WNM) to be improved independently without one negatively affecting the other. However the additional transistors lead to a substantial area overhead. Going the other direction, a 5-transistor (5T) bitcell [4] uses asymmetric sizing to improve RSNM without the area overhead. However, this suffers from degraded WNM when compared to the conventional 6T, and requires an additional voltage used with an assist method for successful write.

We propose an asymmetric 6T (Figure 1) that improves both RSNM and WNM for the same bitcell area as a conventional 6T. The cell has two word-lines and is accessed by a two-phase single-ended write and a single-ended read operation. The cell in Figure 1 is one specific implementation of a 6T bitcell that combines asymmetric sizing, two-phased write and single-ended operation. We describe these ideas in the next section before presenting the specific example of our bitcell.

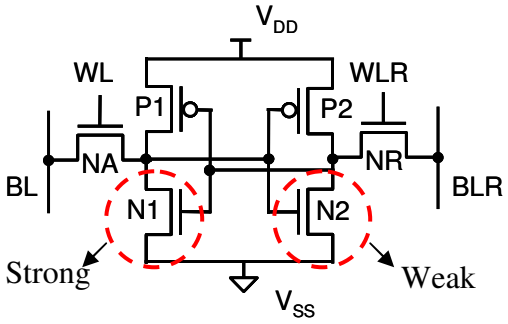

Figure 1: Proposed asymmetric 6T bitcell

An asymmetric 6T with a single word-line (WL) was proposed in [5] that improves both RSNM and WNM at the cost of area. This cell is highly susceptible to half-select related failures (e.g. the cells that are on the activated WL, but whose columns are unselected). The authors overcome this problem by using a fine-grained bitline segmentation scheme, which ensures that the disturb period is small. Thus the probability of an upset reduces. However, this scheme affects the area efficiency of the array due to the increased number of local write and read circuits. The asymmetric 6T that we propose has dual word lines that ensure that the RSNM for all disturbed cells during a read is improved relative to an iso-area symmetric 6T.

In addition to higher RSNM and WNM than an iso-area conventional 6T bitcell, our cell also provides increased read current (I_{READ}) and thus faster discharge of the bitline (BL) during a read. However, since the cell is single-ended, it is a challenge to translate the improvement in I_{READ} into an improvement in performance in terms of overall read access time. This is because logic-gate based full swing sensing that is used for single-ended cells is slower than differential sensing [6]. Thus, we propose a sensing scheme for our single-ended cell that can perform comparably to differential sensing. Further, this scheme can be applied to any single-ended cell.

To summarize, the primary benefits we propose are

- An asymmetric 6T bitcell and a sizing approach that results in a higher mean and lower variability in the

RSNM, WNM, and I_{READ} compared to an iso-area conventional symmetric 6T, allowing for improved V_{MIN}.

- A pseudo-differential sensing scheme for this bitcell that can be extended to any single-ended bitcell, enabling improved performance while maintaining robustness.

The rest of the paper is organized as follows. In section 2, we present the asymmetric 6T bitcell and describe our sizing approach. In section 3, we compare our bitcell to the conventional 6T in terms of noise margins, read current, and leakage. We also compare the half-select RSNM for our cell with the conventional 6T cell. In section 4, we present the sensing scheme that we use and compare it with differential sensing in terms of total read delay. We also examine the impact of variation on our sensing scheme. Finally, we conclude in section 5.

2. Proposed dual word-line asymmetric 6T bitcell

2.1. Increasing the noise margins

Our proposed cell improves on previous asymmetric designs. For instance, asymmetric sizing of the cross-coupled inverters improves RSNM in a 5T bitcell [4]. Figure 2 indicates how the inverters need to be skewed relative to the reference conventional 6T to improve the RSNM. However, the asymmetric 5T cell in [4] has a smaller WNM compared to the conventional 6T, and a combination of write assists need to be used to achieve comparable WNM as the 6T. Instead of using assist techniques to solve the write problem, we add a reset transistor to the bitcell that resets the node QB to '0' before the write cycle, which writes a '1' to the cell, similar to [7]. However, as shown in Figure 3, the cell in [7] requires all cells in a row to be reset at once. It also does not use asymmetric sizing, thus failing to capitalize on the RSNM benefits of the asymmetric structure. We modify this scheme so that the cell reset can be performed without having to reset the entire row, while exploiting the benefits of asymmetric sizing.

Figure 4(a) shows a generalized version of our proposed asymmetric 6T bitcell. The gate of the reset transistor, NR, is controlled by RSTG and the source by RSTS. RSTS is pre-charged high and RSTG is held low. As shown in Figure 4(b), before a write, RSTS pulses low and RSTG pulses high and thus resets the cell to a '1'. RSTG and RSTS can be shared row-wise and column-wise, respectively, or vice-versa, and

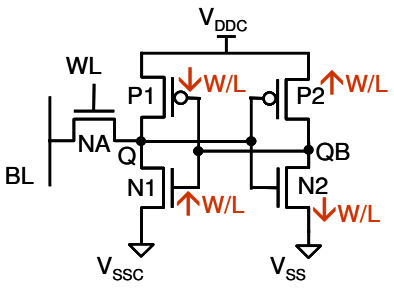

Figure 2: 5T SRAM [4]. Making inverter P1-N1 n-strong and P2-N2 p-strong increases the RSNM.

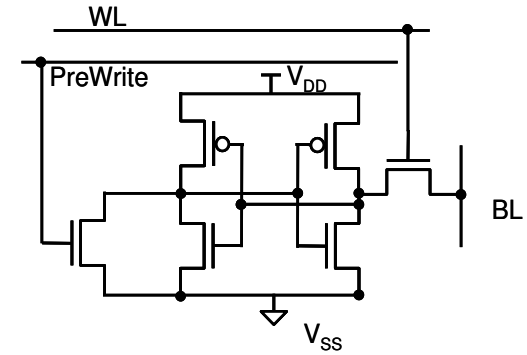

Figure 3: "5T" SRAM with reset [7]. "PreWrite" resets all the cells on a row that share this signal.

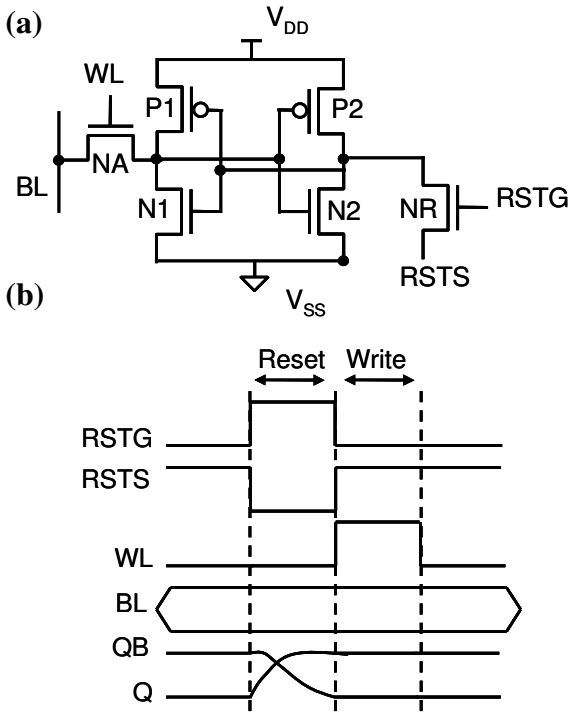

Figure 4: (a) Proposed cell reset scheme. (b) Timing diagram for cell reset and write

activated only for those rows and columns in the array that contain the accessed cell (see Figure 5). This eliminates the need to reset an entire row.

If RSTG and RSTS are routed as shown in Figure 5(a), the cells on the same column as the accessed cell are in a half-selected state during the reset operation. On the other hand, the cells on the same row as the accessed cell are in a half-selected state, if the reset signals are routed as shown in Figure 5(b). Though the routing method chosen does not affect the functionality, it has an impact on the area of the cell as we will discuss in the next section.

Finally, asymmetric sizing can provide significant increase in RSNM (48% in [4]). In our cell, we trade off the improvement in RSNM with WNM by upsizing the access transistors, NA and NR.

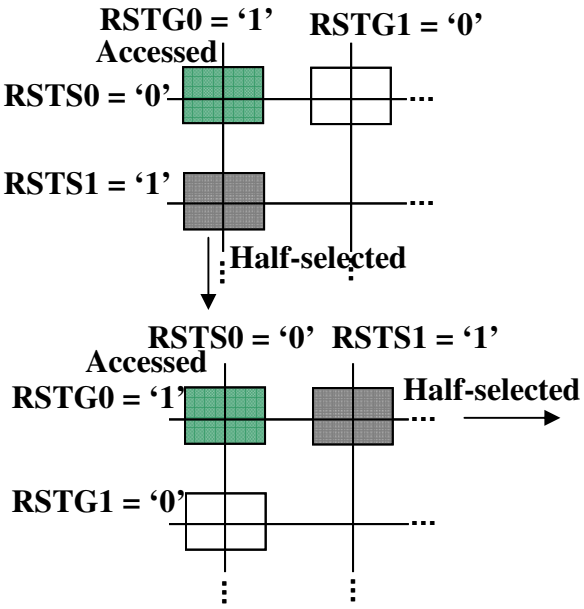

Figure 5: Options to share RSTG and RSTS for the reset transistor (a) column and row-wise (b) row and column-wise

2.2. Sizing for iso-area

Area is an important consideration when designing an SRAM bitcell due to the large number of repeated cells. Because of this, our approach is to maintain a bit cell size as close as possible to a conventional 6T cell.

As described earlier, there are two options to route the signals that control the reset transistor, within an array. The scheme in Figure 5(a) increases the area of the cell even if we choose the same device sizes as the conventional 6T. This is because the RSTG contact that is analogous to a WL contact in the conventional 6T cannot be shared with an adjacent cell on the same row, as in the conventional 6T. Similarly the RSTS contact that is analogous to a BLB contact cannot be shared with an adjacent cell in the same column. This increases the bitcell width and height by the minimum distance that needs to be maintained between two polysilicon

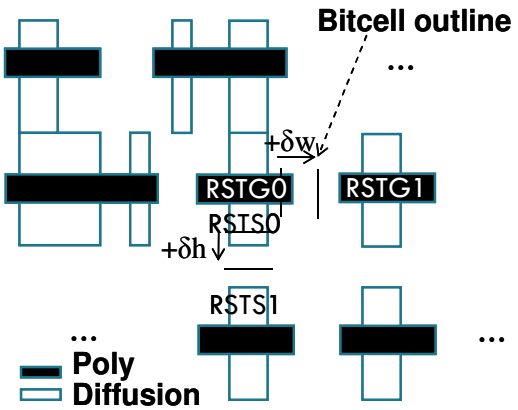

Figure 6: Layout diagram for asymmetric 6T with RSTG and RSTS routed column and row-wise respectively

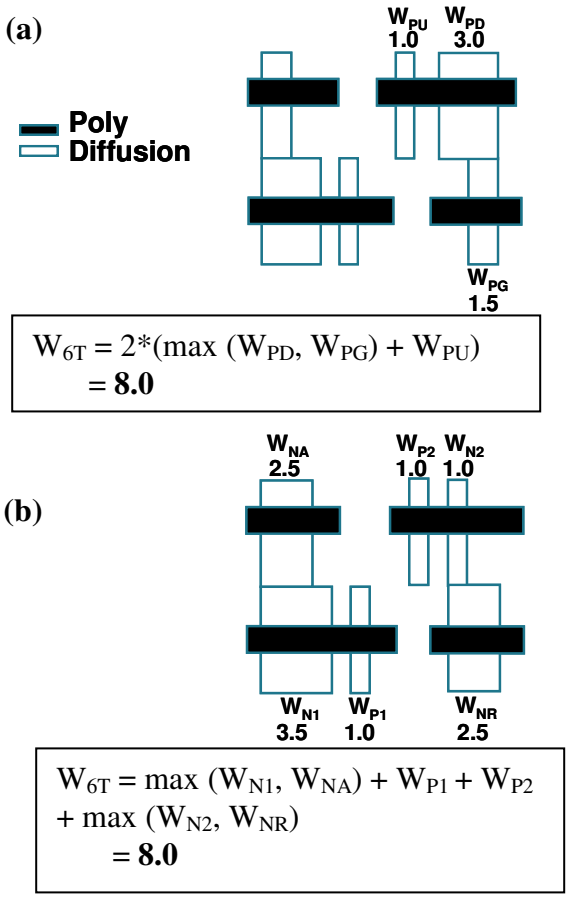

Figure 7: Layout diagram and Normalized device widths for (a) 6T bitcell (b) Asymmetric bitcell

and diffusion regions (δw and δh respectively in Figure 6). We selected the scheme in Figure 5(b), which enables the RSTG and RSTS nodes to be shared similar to a WL and BL respectively, as in a conventional 6T.

As the schematic in Figure 1 shows, we rename the nodes RSTG and RSTS to WLR and BLR respectively, since they are routed similar to a WL and BL of a conventional 6T. We now describe our sizing scheme that enables us to keep the same area as the reference 6T. Figure 7 shows the layout of a conventional 6T bitcell and our asymmetric 6T. We did not change the lengths of any transistors since the commercial sub-45nm technology that we used did not allow it. Thus, the height of the two cells remains the same. For the conventional 6T, N1 and N2, P1 and P2, NA and NR are the same.

First, we make the inverter P1-N1 n-strong by increasing W_{N1} relative to the reference 6T. We also size up the access transistor NA but keep it smaller than N1. Next, we reduce W_{N2} to the minimum width, which makes P2-N2 p-strong. This skewing of the cross-coupled inverters improves RSNM as described in [4]. Finally, we increase W_{NR} so that the reset pulse can be of short duration. W_{NR} is increased so that the width of the cell doesn't exceed the width of the reference 6T, thus ensuring that the area of our cell is the same as the reference 6T. In order to facilitate area comparisons, we did not use "pushed rules" (SRAM-specific DRC waivers) in

either the reference or the asymmetric cell. We believe that, if pushed rules are used, the area reduction will be the same for both the asymmetric and the conventional cells.

3. Comparison with conventional 6T

3.1. Noise margins and V_{MIN}

Figure 8a-b show simulation results in a commercial sub-45 nm technology for the mean RSNM and WNM of our bitcell and the conventional 6T. The RSNM is the side of the least square that can be embedded in the lobes of the butterfly curve [8]. WNM is calculated by using a DC sweep of the WL [9]. The mean values of the noise margins improve across various corners and also at a lower voltage (0.7V). The mean RSNM improvement ranges from 10% to 22%, while the WNM improvement ranges from 2% to 29%, for the process corners and voltages shown below. This improvement is obtained for the same bitcell area as the conventional 6T.

Sizing up the access transistors has the additional benefit of reducing the variability of the WNM. As Figure 8c-d show, the σ/μ of the WNM is lower than that of the conventional 6T across different process corners and voltages, with a reduction of 36% at the FF corner, for the write '0' case at 1V.

On the other hand, the σ of the RSNM for the asymmetric cell is more than that of the conventional 6T. This is because, for the symmetric 6T, the RSNM is the minimum of the RSNM of the two half-cells, but it is the RSNM of the stronger side for the asymmetric cell. Since the σ of the minimum of two distributions is less than the σ of each of them, the resulting distribution of the final RSNM is wider for

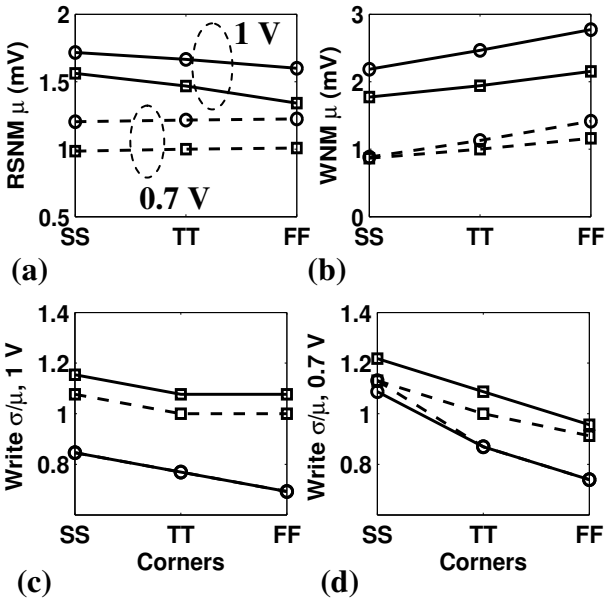

Figure 8: Normalized Mean (a) RSNM and (b) WNM, and normalized σ/μ of WNM at (c) 1 V and (d) 0.7 V at various process corners and voltages from a 1000 point Monte Carlo (MC) simulation. In all the plots, the circular and the square markers represent the asymmetric cell and the conventional 6T respectively. In (c) and (d), the solid and dashed lines represent the write '0' and '1' cases respectively.

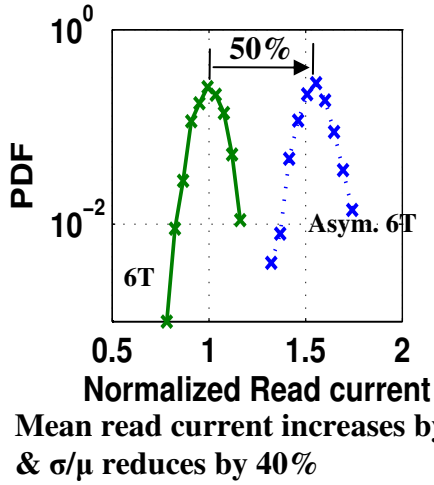

Figure 9: Read current for 6T and asymmetric cell @ 1V, TT, and 27 ^{0}C from a 1000 point MC simulation.

the asymmetric cell. However, the RSNM of the asymmetric cell can never be worse than that of the symmetric 6T. This results in a wider distribution with a higher mean for the asymmetric 6T, but the tail of this distribution doesn't go beyond that of the symmetric 6T distribution. This is discussed further in section 3.3.

The larger noise margins result in a smaller V_{MIN} for our cell. We define the Read (Write) V_{MIN} for a bitcell as the minimum V_{DD} at which the cell can read (write) successfully. The Read (Write) V_{MIN} for an array is the maximum of the bitcell Read (Write) V_{MIN}. For a 1000 sample Monte Carlo simulation, we find the Read V_{MIN} for the asymmetric 6T to be 21.5% smaller and the Write V_{MIN} to be 4% smaller than the conventional 6T at the TT process corner.

3.2. Read Current

The wider pull-down and access transistors lead to an increase in read current. As Figure 9 shows, the mean read current increases roughly by 50% for the sizes chosen in our implementation. In addition, the variability of the read current in terms of σ/μ also reduces by 40% due to the larger access devices. This is a significant benefit when designing large memories, since the designer needs to look farther out in the tail of the distribution. However, this improvement in read current can be translated to a corresponding improvement in total read delay only if a single-ended sensing scheme that is as fast as differential sensing is used. We propose such a sensing scheme in Section 4.

3.3. Half-select stability

Half-selected cells are defined as the cells on the activated word-line whose bitlines are not activated (e.g. remain in the pre-charged state and not pulled low). The stability of these cells is reduced when compared to an unaccessed cell, both during read and write. An asymmetric 6T cell with similar sizing but a single WL has a worse half-select RSNM during both read and write. Figure 10 shows the half-select state during read and write for both these bitcells. For both the asymmetric cells, due to the skewed sizes, the half-cell not

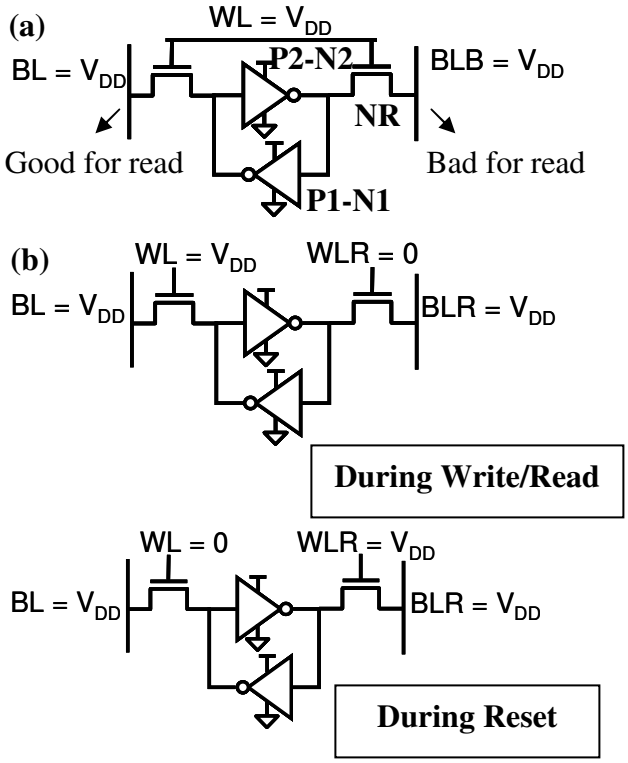

Figure 10: Half-selected cell for (a) single WL and (b) dual WL asymmetric 6T

involved in the read (e.g. P2-N2-NR in our case) is weaker than the half-cell of the conventional 6T, and is more susceptible to flipping. However, with the dual word-line scheme, NR is turned off during a read and the half-select RSNM is the RSNM of the stronger side (e.g. P1-N1-NA). Thus we reduce the half-select issue during a read when compared to a single-WL asymmetric cell as well as a conventional 6T. As shown by the distributions in Figure 11, the mean RSNM for half-selected cells during read improves by 18% under nominal operating conditions. The spread of the distribution increases, but the RSNM of the asymmetric 6T is always greater than that of the conventional 6T, due to the reasons described in section 3.1.

However, as Figure 10 shows, the problem still remains during reset. We can get around the half-select problem by writing the entire row or by using a read-modify-write technique [1]. Thus an alternative implementation of our proposed bitcell would involve using a single WL, while keeping the same device sizes, and use one of the above approaches to solve the half-select issue. Another solution would be to make NR weaker by using a higher V_T device or by reducing its width. Since the half-cell P2-N2-NR is already sized for write, we need not make NR as wide as NA. While this would also reduce the cell area, we chose not to do this since it would reduce the gains in write margin for the write '1' case and worsen the impact of variation.

3.4. Cell leakage

Figure 12 shows the leakage of the asymmetric 6T and the conventional 6T versus the supply voltage. The asymmetry causes our cell to have data-dependent leakage. However, the

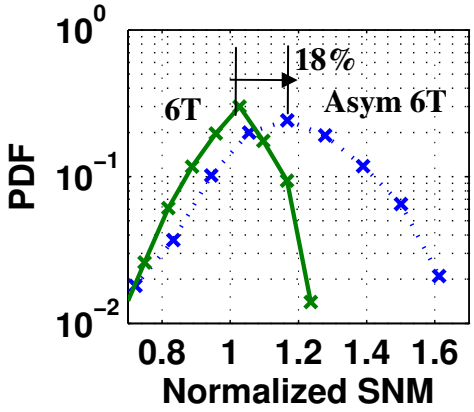

Figure 11: Half-select cell RSNM during read for conventional 6T, and asymmetric 6T @ 1V, TT, and 27 ^{0}C from a 1000 point MC simulation

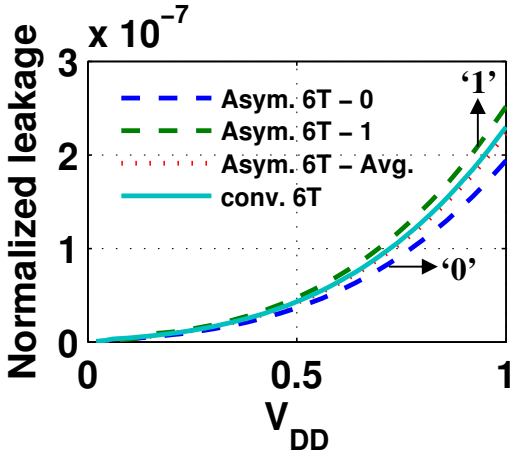

Figure 12: Standby cell leakage for conventional and asymmetric 6T

average leakage of the asymmetric cell is nearly the same as that of the conventional 6T at any particular voltage. Moreover, the increased robustness of the asymmetric 6T cell enables a lower V_{MIN}, which implies that the asymmetric 6T array would have a lower standby leakage than a conventional 6T array when operating under V_{MIN} conditions. We further observe that the leakage of a cell storing '0' is less than that of the conventional 6T by 10-15%, due to the smaller size of the leaking pull-down (N2). Since SRAM caches tend to store more number of 0s than 1s [10], the leakage power of the asymmetric 6T array at a given operating voltage could potentially be less than that of a conventional 6T.

4. Single-ended sensing using a split BL

As described earlier, to leverage the improvement in cell read-current, a single-ended sensing scheme that results in overall read access time comparable to differential sensing is required. We describe such a scheme in this section.

4.1. Proposed single-ended sensing scheme

We propose a split bitline sensing mechanism for reading our single-ended asymmetric 6T bitcell. Figure 13 depicts this

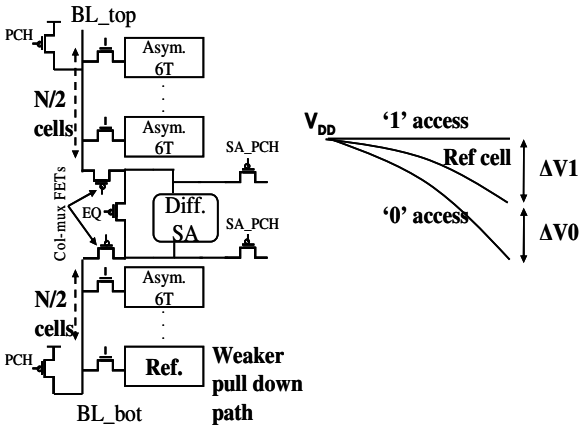

Figure 13: Single-ended sensing using a split BL.

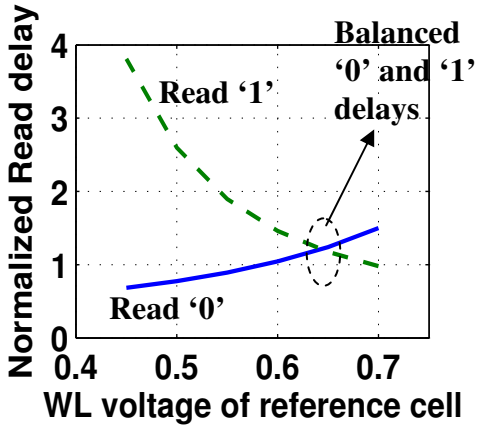

Figure 14: Impact of reference WL voltage on read '0' and '1' delays

scheme. The array is split in two halves and the sense amplifier (SA) is placed in the middle. We use a latch-type voltage SA that is used for conventional 6T bitcells. The top and bottom half of the array each contain a single row of weaker cells (with lower read current than the regular cell). This is used as the reference for the differential SA. A similar idea was described in [11] for single-ended sensing in a DRAM, where a storage capacitor with half the capacitance as the normal cell was used as the reference. The row containing the reference cells can be a part of the array or additional to the array. In Figure 13, the reference cells are shown in an extra row, and only the bottom reference cell is shown.

The sensing works as follows. Without loss of generality, we assume that the cell being read is in the top half of the array. The WL of the accessed row is activated, along with the WL of the reference row on the opposite side of the SA. If the cell being read stores a zero, it discharges the corresponding BL faster than the reference cell, as shown by the curve marked '0' access in Figure 13. On the other hand, if the cell being read stores a high value, the BL does not discharge, as indicated by the curve marked '1' access in the figure. The reference cell on the other side discharges as before. Thus, an appropriate differential is developed, which is quickly resolved by the SA. Note that the output of the SA would need to be inverted if the accessed cell was in the other half of the array.

In this scheme, in addition to an increase in read current, the bitline capacitance is reduced due to half the number of cells on the bitline. This helps compensate for the fact that the BL needs to be discharged twice as much as in the case of the conventional 6T (assuming the reference cell is half as strong as the normal cell) to generate the same net differential for the SA.

To reduce the strength of the reference cell, we use a lower WL voltage, which reduces the cell I_{READ}, thus weakening the cell. This involves the overhead of generating the extra voltage and switching to it when performing a read. Alternatively, we can use a reference cell that is sized so that its I_{READ} is less than that of the regular cell (e.g. by weakening NA or NR). This eliminates the need for an extra voltage, but the reference bitcell now involves additional design effort and also leads to an area overhead since separate edge cells are required for the reference cell. We chose the former method of creating the reference cell rows due to its ease of implementation and testability.

The WL voltage chosen for the reference cell affects the differential development for the '0' and '1' cases in opposite ways. As Figure 14 shows, as the WL voltage of the reference cell is reduced, the read '0' delay decreases due to faster differential development between the read and the reference bitlines. On the other hand, the read '1' delay increases due to the slower discharge of the reference bitline. Thus, there is an optimal point for the reference WL voltage which balances the read '0' and '1' delays.

4.2. Comparison with Differential Sensing

4.2.1. Nominal Read Delay Comparison

We use the schematics shown in Figure 15 for comparing the split BL sensing scheme with differential sensing. Read delay is typically defined as the time elapsed between the WL reaching 50% of the full-rail high value and the output of the SA reaching the resolved full rail value. In our setup, the capacitance seen by the input nodes of the SA is the same for both sensing schemes, since we do not alter the sizes of the column-mux or the SA precharge and equalize devices. Further, we use identically sized SAs in both setups. Thus, if we assume that the SA resolution delay is the same, the read delay can be compared by simply comparing the time taken to develop a fixed bitline differential.

Figure 16 shows the nominal bitline differential development delay for the two sensing schemes, for different column heights. The "cells per bitline" on the x-axis in this figure refers to the total height of the array. Thus, for example, 32 cells per bitline would mean the split BL sensing has 16 cells in the top and bottom halves of the array (see Figure 13). In both cases, one SA is shared by 32 cells. For both the sensing schemes, we arbitrarily choose 150 mV as the required differential before the SA is enabled. We observe that the mean read delay of the split BL case is comparable to that of the differential sensing for shorter bitlines, but is

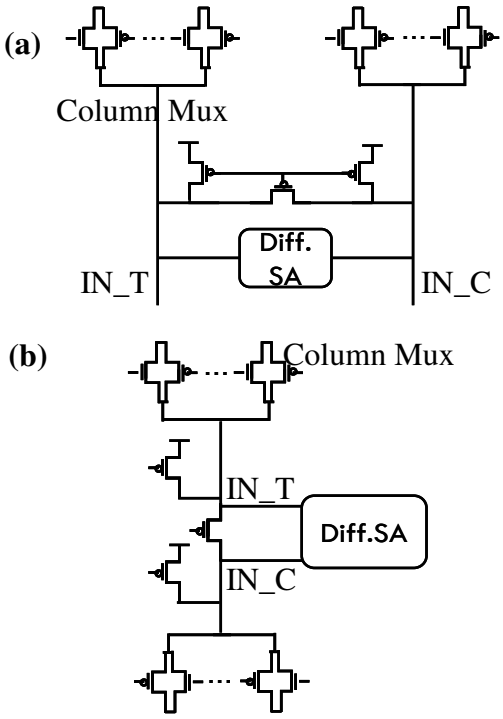

Figure 15: Schematics for comparing (a) differential and (b) split BL sensing

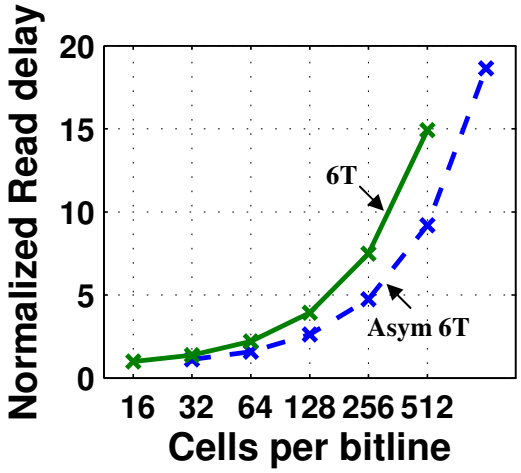

Figure 16: Normalized access times for 6T with differential and asymmetric 6T with split BL

significantly lesser for longer bitlines (e.g. 38.3 % lower mean delay for a 512 long bitline).

However, increased bitline leakage due to longer bitlines and the impact of variation makes shorter bitlines more attractive. This is discussed in the next sub-section.

4.2.2. Impact of variation

We now consider the impact of variation on the split BL sensing scheme. Since the reference voltage depends on the I_{READ} of the reference cell, variation in this cell, as well as bitline leakage, can cause the distributions of the SA input voltages to overlap. This leads a '0' and '1' to be indistinguishable. In conventional sensing on the other hand,

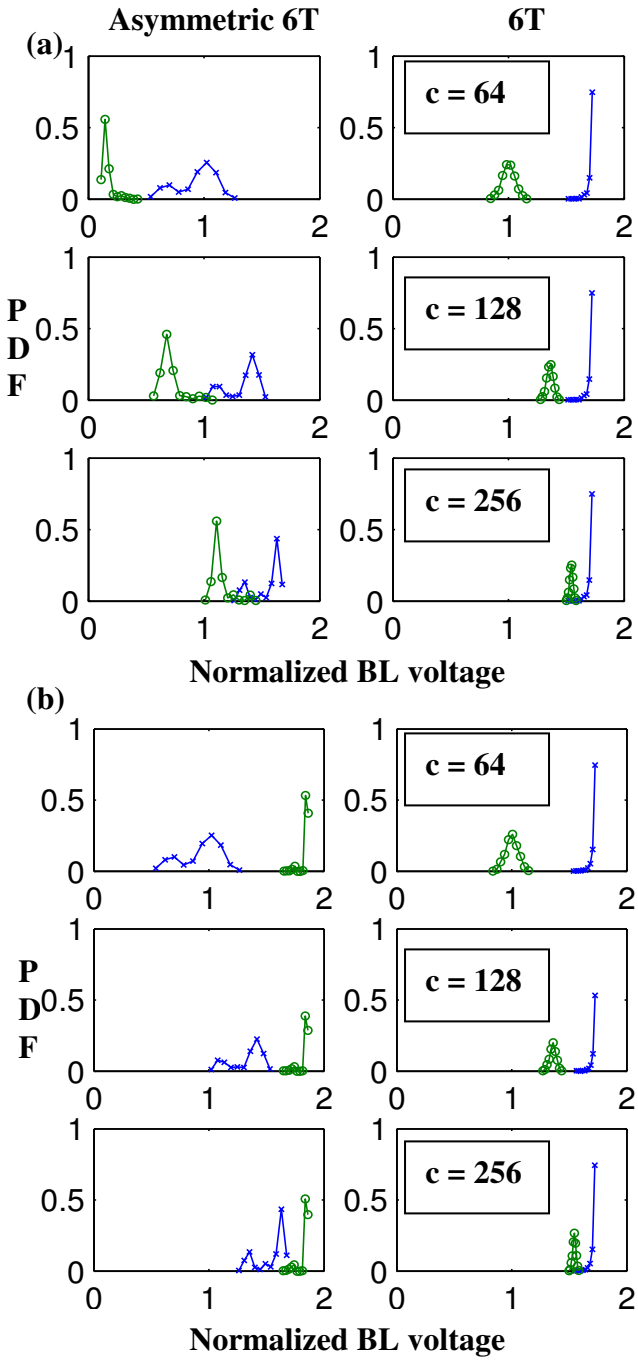

Figure 17: SA input distributions for (a) Read '0' (b) Read '1'. The distributions with the circular and cross markers are associated with the sensed and reference BL voltages respectively.

the variability of the reference voltage is only due to bitline leakage.

Figure 17 shows the distributions of the SA inputs (IN_T and IN_C in Figure 15), for a fixed WL pulse, and fixed reference voltage for the split BL method. The distributions are shown for three different column heights (c = 64, 128 and 256) and for both read '0' and '1' cases. The column height here refers to the number of cells on the discharging BL. Thus, in the split BL case, the total height of the array is 2c, while it is c for the differential sensing case.

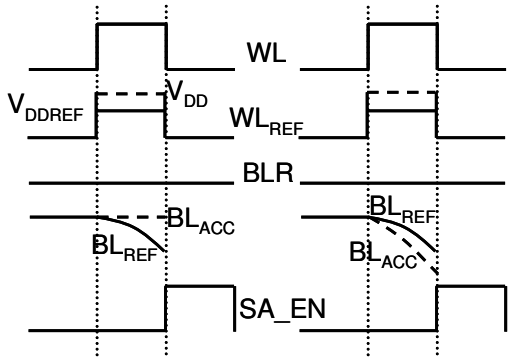

Figure 18: Timing diagrams for read

We observe that as the height of the column increases, the overlap between the sensed and reference voltage increases, causing the SA output to be unreliable. However, for shorter column heights, as is the norm in modern SRAM designs, the distributions of the sensed and reference voltage are wide apart. This is because the higher drive strength and lower BL capacitance pulls the two distributions away from each other. Thus, the split BL sensing works though the reference has higher variability when compared to conventional sensing.

We now describe the read operation (Figure 18) for the proposed bitcell. The WL of the accessed cell (WL_{ACC}) and that of the reference cell (WL_{REF}) go high. WL_{REF} only goes up to V_{DDREF}, which is lower than V_{DD}, to reduce the read current of the reference cell. Note that '0' must be written to all the reference rows for the sensing to work. Now an appropriate differential develops, as described previously. Once sufficient differential is developed to overcome SA offset and strobe (SA_EN) delay variation, the differential SA is fired and resolves to the value stored in the cell.

5. Conclusion

We have presented an asymmetric 6T bitcell that has higher RSNM and WNM than the conventional 6T for the same bitcell area, and reduced variability in WNM (in terms of σ/μ). In addition, it provides higher read current with lower variability. We have also proposed a single-ended scheme using a split BL that uses a weak cell as a reference and described its implementation. This scheme provides a 38% higher mean macro read delay for a long bitline, but is more impacted by variation than differential sensing. From simulations in a commercial sub-45nm technology, the asymmetric cell allows for a 21.5% reduction in Read V_{MIN} and a 4.1% reduction in Write V_{MIN} versus a conventional 6T cell. We don't anticipate the Standby V_{MIN} to degrade since the hold static noise margin does not worsen due to asymmetric sizing, as shown in [4].

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7. References

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