Asymmetric sizing in a 45nm 5T SRAM to improve read stability over 6T

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Outline

• Motivation and related work
• 5T bitcell
• Asymmetric sizing
• Writing to the 5T
• Measured results
• Conclusions
Motivation

• Low-power $\Rightarrow$ lower $V_{DD}$

• *But* lower $V_{DD}$ means…
  - Reduced noise margins
  - Increased variability ($\sigma$)

• Unfavorable trade-offs limit 6T scalability
  - Performance vs. density vs. stability/yield vs. power
  - Read vs. write

• Need a solution that allows better trade-offs
Related work

• Several existing alternative bitcells –
  ➢ 8T (Chang07) –

  ➢ Earlier 5T bitcells (e.g. Carlson04)
    ➢ no asymmetry or asymmetry to improve write alone
    ➢ variation upsets delicate balance

Area overhead
Problem 1: Single-ended sensing

Proposed 5T bitcell: Read

Read ‘0’

Read ‘1’
Proposed 5T bitcell: Write

Problem 2: Single-ended write ‘1’

Write ‘0’
Improving RSNM

Asymmetric sizing increases RSNM

6T Read SNM

“6T like” 5T Read SNM

Smaller lobe limits RSNM
Asymmetric sizing options

p-strong
E.g. Decrease $W_{N2}$

n-strong
E.g. increase $W_{N1}$, $L_{P1}$

Sizing to keep same area as 6T
Asymmetric sizing options

1. RSNM
2. WNM (with assist)
3. Delay
4. Lkg

Inc. $W_{N1}$, Dec. $W_{N2}$, (both)
Dec. $W_{P1}$ (5T3)

N1 stronger $\Rightarrow$ lower delay but lower WNM
Asymmetric sizing options

1. RSNM
2. WNM (with assist)
3. Delay
4. Lkg

Inc. \( L_{P1}, W_{N1} \)

P1 weaker \( \Rightarrow \) less RSNM, WNM better
Asymmetric sizing options

1. RSNM
2. WNM (with assist)
3. Delay
4. Lkg

- Inc. $W_{N1}, L_{P1}$ (5T2)
- Inc. $W_{N1}, L_{N2}$ (5T5)

Longer lengths ⇒ less lkg, lower $\sigma$
Layout and area

Abutted 6Ts

Abutted 5Ts – save area

Abutted 5Ts – increase margins for same area
Example: 5T with wider N1

Half-select RSNM improves

RSNM

Delay

µ ↓ 13.4%

σ ↓ 13.4%

1000 MC @ 1 V, TT, 27 °C

PDF

SNM (mV)

10^0 10^-1 10^-2 10^-3

0 200 400

HSNM

6T

5T

10^0 10^-1 10^-2 10^-3

20 30 40
Writing to the 5T

Cannot pass a “strong” 1

stronger than NA

W. Assist - Collapse $V_{DDC}$

Row-wise or column-wise $V_{DDC}$
Test chip architecture

32 kb 5T
16 kb 6T
4 kb banks
Measurements – Impact of sizing on write-ability

sizing 1 – widen N1
sizing 2 – lengthen P1, N2

Asym. sizing to improve writability

$V_{DD} = 1 \text{ V}$

Zero errors
Measurements – WL boost to improve write

- WL boost ⇒ less errors for same $V_{DDC}$ drop

Combine Write assists to improve write-ability

- $V_{DDC} = 0.5 * V_{DD}$
- WL = 1.2 * $V_{DD}$

Graph showing bit error rate with different $V_{DD}$ values and WL voltages.
Conclusions

• 5T cell with asymmetric sizing proposed.
• Improves RSNM.
• Sizing knob to trade-off performance, area and noise margins.
• Write-ability recovered through assists.
• 45nm test chip demonstrates functionality.
Questions?