A 150nW, 5ppm/^{o}C, 100kHz On-Chip Clock Source for Ultra Low Power SoCs

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***Abstract*-This paper presents an ultra low power clock source using a 1µW temperature compensated on-chip digitally controlled oscillator (Osc_{CMP}) and a 100nW uncompensated oscillator (Osc_{UCMP}) with respective temperature stabilities of 5ppm/^{o}C and 1.67%/^{o}C. A fast locking circuit re-locks Osc_{UCMP} to Osc_{CMP} often enough to achieve a high effective temperature stability. Measurements of a 130nm CMOS chip show that this combination gives a stability of 5ppm/^{o}C from 20^{o}C to 40^{o}C (14ppm/^{o}C from 20^{o}C to 70^{o}C) at 150nW if temperature changes by 1^{o}C or less every second. This result is 7X lower power than typical XTALs and 6X more stable than prior on-chip solutions**

I. INTRODUCTION

Wireless sensor nodes and body sensor nodes (BSNs) require ultra low power (ULP) hardware to support long system lifetimes on stringent energy budgets. These nodes typically require a stable clock source for precise data sampling, an RF modulation clock, and keeping time to reduce the cost of re-synchronizing to other radios. The conventional approach of using a crystal oscillator (XTAL) adds 3-4 off-chip passives, has startup times in the ms to second range, and can consume an appreciable fraction of the system power. For example, the energy harvesting BSN SoC in [1] consumes 19µW while measuring ECG, extracting heartrate, and sending RF packets every few seconds, and over 2µW of that total is in the 200kHz XTAL. The alternative clocking scheme to replace XTAL with low power and low cost on-chip reference oscillators for low power systems is an ongoing effort [2-5]. Widely varied approaches exist. In [5], authors present a CMOS relaxation oscillator. High temperature stability is achieved using poly and diffusion resistors together to realize the resistor in an RC relaxation oscillator. These resistors have complementary temperature dependence, and they cancel the effect of temperature variation to achieve a temperature stability of 60ppm/^{o}C. On-chip oscillators using the gate leakage current have been proposed in [2-4]. Gate leakage current has very small temperature dependence, which makes these oscillators stable. However these oscillators can operate only at very low frequency (0.1-10 Hz) owing to the low magnitude of gate-leakage current. Also the oscillation frequency is not very well controlled across process. The most stable oscillator [4] in this category has a temperature stability of 32ppm/^{o}C operating at 0.4Hz. In this paper, we present a new scheme to replace XTALs with an ULP on-chip clock source (no off-chip passives) for the ~100kHz range that is roughly 7X lower power than XTALs and has a temperature stability of 5ppm/ ^{o}C.

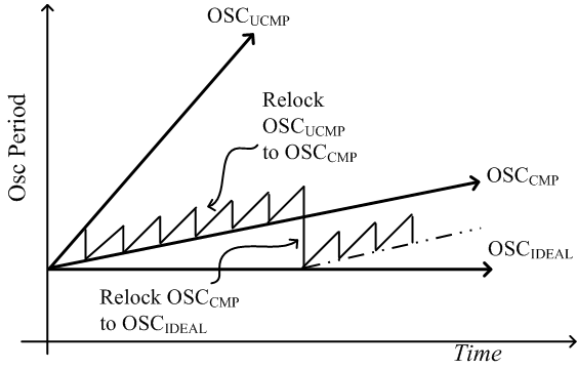

Fig. 1. Scheme of re-locking low stability oscillator to achieve high effective stability

II. ULP ON-CHIP CLOCK SOURCE

To maintain a stable on-chip clock source, we need a compensated oscillator (Osc_{CMP}). However, these circuits tend to consume power comparable to XTALs, in the few µW range for ~100kHz. We propose a scheme to use an ULP uncompensated oscillator (Osc_{UCMP}) with the Osc_{CMP} to provide both stability and ULP consumption. Fig. 1 shows the concept. As temperature changes at a given rate, both oscillators will aggregate time error relative to the ideal reference, with Osc_{UCMP} accumulating error much faster due to its lower stability. If we periodically lock Osc_{UCMP} to Osc_{CMP}, then its effective stability stays within a bounded error relative to Osc_{CMP}, and we can make this error arbitrarily small by changing the duty cycle of re-locking. We can also re-lock to the original reference if it is available (e.g. XTAL or signal over RF). In between lock points, the higher power oscillator(s) can shut down, setting the system power to that of the Osc_{UCMP}. To make this work well, we need a fast locking circuit, low power oscillators with rapid turn on/off, and digital calibration storage. Fig. 2 shows the architecture of our clock source.

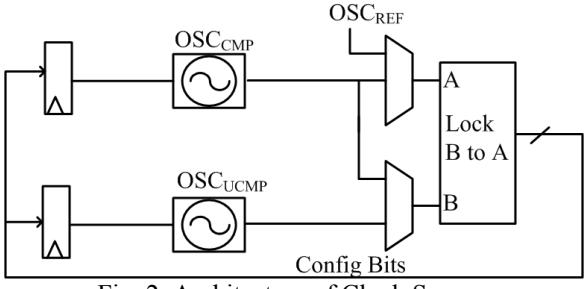

Fig. 2. Architecture of Clock Source

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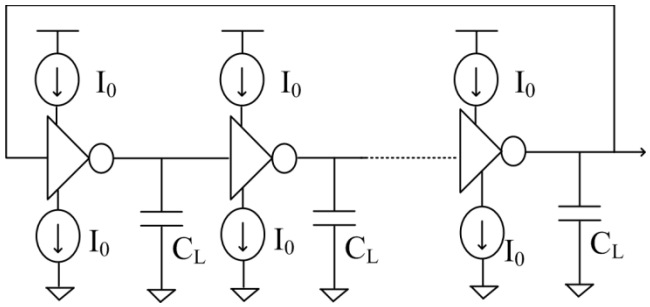


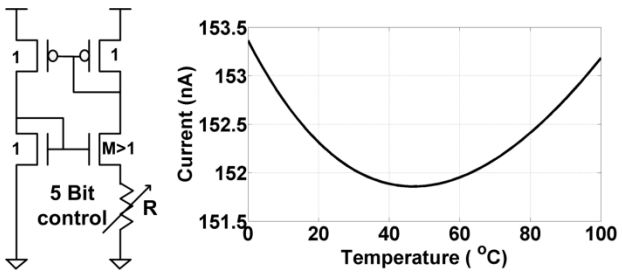
Fig. 3. Current controlled Ring Oscillator

III. COMPENSATED OSCILLATOR

Our Osc_{CMP} uses a current controlled ring oscillator. Fig. 3 shows the circuit diagram. It is designed to be stable across temperature, and it uses configuration bits to compensate for process variation. Its oscillation frequency is set by current I_o and capacitance C_L, which are MIM caps with very small temperature variation. To set the constant current I_o, we use a PTAT and CTAT current source. Fig. 4a shows the PTAT current source. The current of a PTAT current source increases almost linearly with temperature. We use a long channel MOS transistor operated in the strong inversion region to implement the CTAT, whose current decreases almost linearly with temperature. We add the current from the PTAT and the CTAT to get a current independent of temperature. Fig. 4b shows that current I_o varies by 1% over a 100°C range (~100ppm/°C).

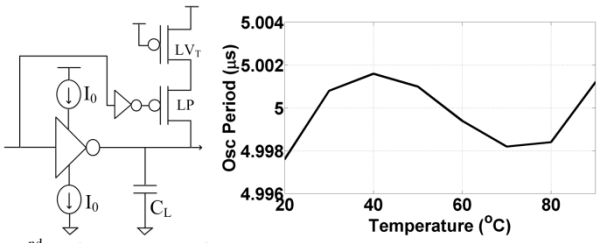
A. *2nd Order Compensation*

The oscillator based on the current source of Fig. 4b will have an oscillation period that will still have a small dependence on temperature. The period of oscillation will reduce as the temperature goes up from 20°C-100°C. We employ 2nd order compensation to further improve stability. This circuit comprises an off, low threshold (LV_T) MOS, a switch, and an inverter. Fig. 5a shows the circuit diagram of the 2nd order compensation. It essentially forms a leakage pull-up path that adds charge to C_L, slightly increasing delay. This slight increase in delay increases with temperature. Fig. 5b shows how this nullifies the 2nd order increase in current at high temperature, giving a nearly flat period for a 200kHz reference over the range of 20°C to 90°C.



a) PTAT b) Simulaton of Constant Current I_0

Fig. 4. a) PTAT b) Sim of PTAT+CTAT Constant I_o



a) 2nd Order Compensation b) Temperature variation of Clock period

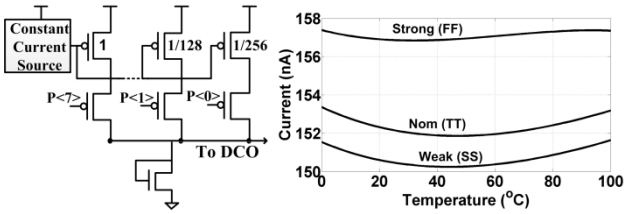
Fig. 5. a) 2nd Order compensation circuit b) Temperature variation in simulation

B. *Process Compensation*

We use configuration bits to compensate the effects of process variation on the constant current source and delay element. In the current source, variation may offset the PTAT and CTAT current so that one dominates in the target frequency range, making temperature stability impossible. We vary resistance R in the PTAT (Fig. 4b) to balance its current with the CTAT against global variation using 5 bits. Similarly we use 6-bit binary weighted off-transistors in the 2nd order compensation to align the leakage current to compensate for the process drift in leakage. We use the constant current source as an input to a binary weighted (8-bit) current mirror (Fig. 6a). This lets us generate the desired current for a given desired frequency across process (e.g., Fig. 6b) at 20ns resolution. We include 10-bit coarse and 5-bit fine control for 1ns and 20ps resolution, respectively, which are set by the locking circuit (Section V). This results in a Digitally Controlled Oscillator (DCO) (Fig. 7) that can lock to a desired frequency.

C. *Power Supply Variation*

The Osc_{CMP} is sensitive to variation in the power supply.



a) Binary Weighted Source b) Process Variation of current

Fig. 6. a) Binary Weighted Source b) Simulation result of current source variation across process

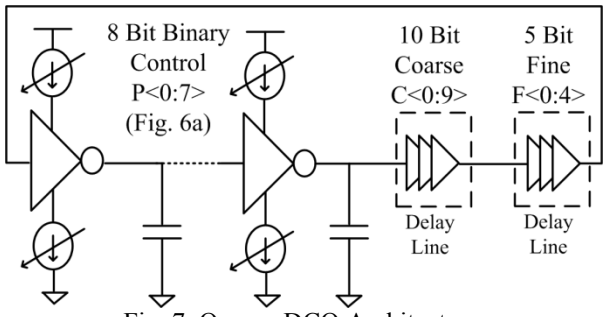


Fig. 7. Osc_{CMP} DCO Architecture

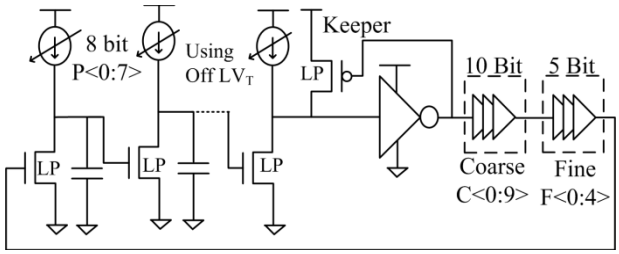


Fig. 8. Osc$_{UCMP}$ DCO Architecture

The PTAT circuit has better power supply tolerance but the CTAT is more sensitive as it uses V_{DD} directly at its gate. Osc$_{CMP}$ shows a dependence of ~0.1%/mV. This is still better than [4] where power supply dependence is 0.42%/mV but it could be a problem for stability if V_{DD} is poorly regulated. Osc$_{CMP}$ will aggregate error over time. This can be addressed either by using low noise regulator such as proposed in [6] or by relocking Osc$_{CMP}$ often with the external references.

IV. UNCOMPENSATED OSCILLATOR

The Osc$_{UCMP}$ uses leakage as the current source to the delay elements along with the same digital inverter-based coarse and fine delay compensation as the Osc$_{CMP}$. It uses binary weighted off LV$_T$ transistors for the realization of the current source. Fig. 8 shows the Osc$_{UCMP}$ architecture. The use of off LV$_T$ transistors gives a lower area DCO at ~100kHz. Long channel transistors are needed to realize it at ~100kHz frequencies with on transistors. This will increase the area significantly. Since no compensation is needed for Osc$_{UCMP}$ we chose the lower area solution. Osc$_{UCMP}$ consumes 80nW of power at 100kHz in simulation. It has a poor temperature stability of 1.67%/^{o}C

V. LOCKING CIRCUIT

We use a 5-bit counter as a frequency comparator to compare Osc$_{CMP}$ to a reference or to compare Osc$_{UCMP}$ to Osc$_{CMP}$. The reference clock (REF_CLK) is divided by 2 and fed to the frequency comparator. The divided clock is called REF. As REF goes high, DCO gets enabled and will start oscillating. The counter starts counting the rising edges of the DCO when the reference input is high. If it counts more than 1, the output of the frequency comparator goes high, else it is low. Fig. 9 shows the timing diagram. Our locking circuit comprises this comparator, SAR logic, and either DCO in a feedback configuration. Fig. 10 shows the architecture of the locking circuit. The frequency comparator gives 1 when the DCO's output frequency is higher than reference and 0 when it is lower. The SAR logic approximates the current and delay inside the DCO based on the logical output of the comparator and sets the 23 DCO control bits, which are stored in a register. The comparison is performed when REF is high, and the current source is configured when REF is low to let the current source settle correctly. Fig. 11 shows the locking transient at 200kHz. The lock takes 46 reference cycles and has a resolution error of ~20ps. Once the calibration is performed, the DCO runs on its own. The temperature compensation scheme controls the drift.

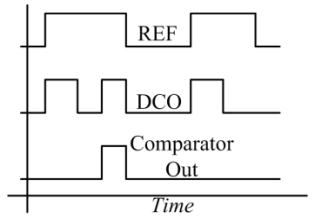


Fig. 9. Frequency Comparator

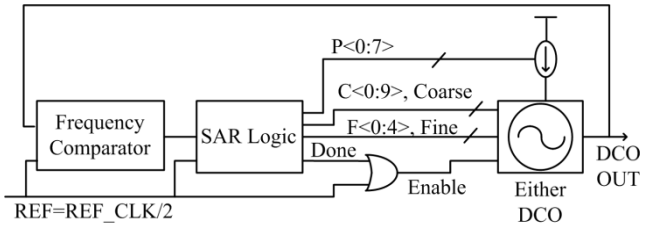
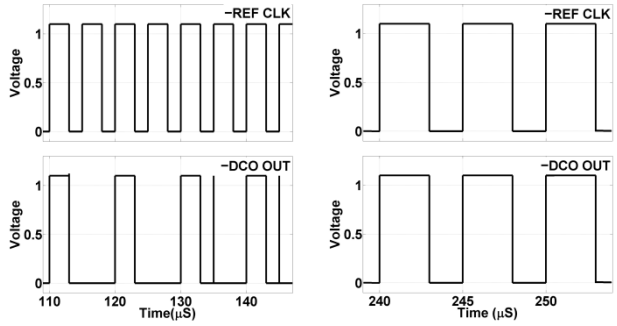


Fig. 10. Fast Locking circuit for DCO using binary search

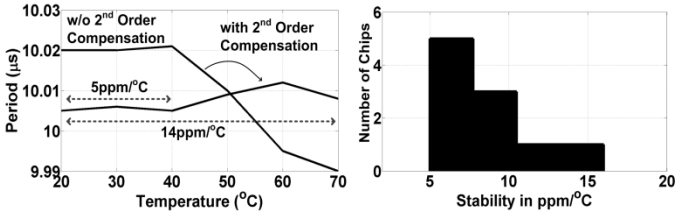


a) Calibration Transient b) Final Output

Fig. 11. Simulation result of Locking transient

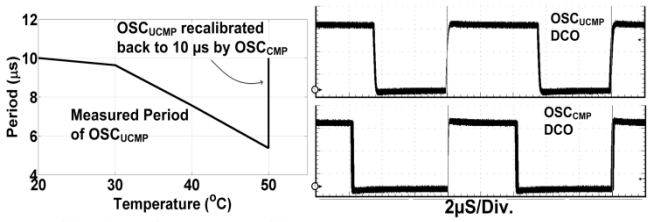
VI. MEASUREMENTS

We implemented the clock source (0.5mmx0.5mm) in 130nm CMOS. Osc$_{CMP}$ and Osc$_{UCMP}$ consume 1μW and 100nW at 100kHz, 1.1V V_{DD}, respectively. The process tuning bits give us a full measured locking range from 15kHz to 350kHz. In this range, we can lock successfully to the reference within the accuracy of jitter on the input clock. Fig. 12a shows the measured stability of the Osc$_{CMP}$ after calibration as 5ppm/^{o}C in a BSN compatible range of 20-40^{o}C (14ppm/^{o}C from 20^{o}C to 70^{o}C). Without the 2nd order compensation, this stability degrades to 60ppm/^{o}C. Fig. 12b shows the temperature stability for 10 chips.



a) Measured Clock period of OSC$_{CMP}$ b) Measured Stability across 10 chips from 20-40 ^{o}C

Fig. 12. Stability Measurements



a) Recalibration of OSC_{UCMP} with OSC_{CMP}

b) Measured Waveform of DCO outputs at 100khz after re-calibration

Fig. 13. Recalibration of Osc_{UCMP} with Osc_{CMP}

We lock Osc_{CMP} to a 100kHz reference, lock Osc_{UCMP} to Osc_{CMP}, then power down Osc_{CMP}. Fig. 13 shows the measurement result of recalibration of Osc_{UCMP} with Osc_{CMP}. In this test Osc_{CMP} was calibrated to 100kHz by an external reference and Osc_{UCMP} was calibrated by Osc_{CMP} at 20°C. After that we shut down Osc_{CMP} and raise the temperature of the measurement to 50°C. Then we wake up Osc_{CMP} and recalibrate Osc_{UCMP} with it. Fig. 13a shows the process, and Fig. 13b shows the output waveform after calibration. Using this scheme, we can achieve stability (5ppm/°C) at ultra-low power. Fig. 14 shows the result of duty cycling for the case when temperature varies by 1°C/s or less. We achieve a stability of 5ppm/°C at 150nW. During locking, we can turn on Osc_{CMP} at the rising edge of Osc_{UCMP} and pass Osc_{CMP} as the clock to avoid glitching or clock gate the system clock to prevent problems in downstream circuits. Fig. 15 shows the die photo. Fig. 16 shows that our work is 10X more stable and consumes 3X less energy than the prior art. Some ULP timers for BSNs are approaching our stability [3-4], but they are 10^6 slower

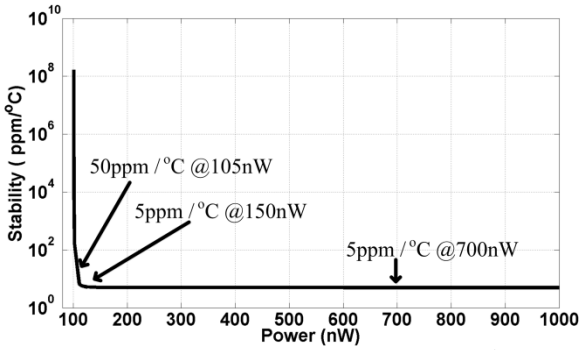


Fig. 14. Measured Power/Stability tradeoff for 1°C/Sec. temperature change

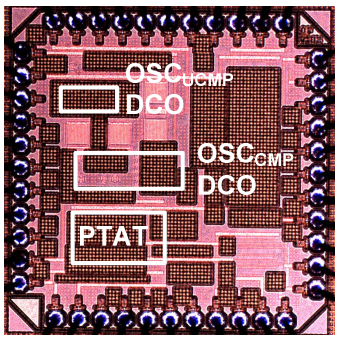


Fig. 15. Die Photo

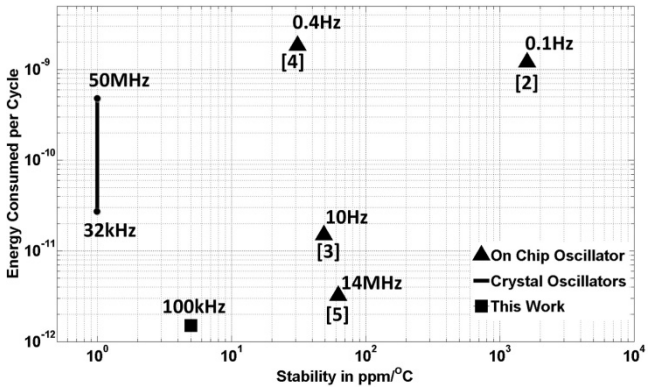


Fig. 16. Energy/cycle and Stability comparison with existing solutions

frequency. We exhibit similar stability to an XTAL with ~7X less power and no off-chip components, providing a low cost ULP solution for wireless sensors and BSNs.

VII. CONCLUSION

We presented an ultra low power clock source using a 1µW temperature compensated on-chip digitally controlled oscillator (Osc_{CMP}) and a 100nW uncompensated oscillator (Osc_{UCMP}) with respective temperature stabilities of 5ppm/°C and 1.67%/°C. We also presented a fast locking circuit that re-locks Osc_{UCMP} to Osc_{CMP} often enough to achieve high effective temperature stability. Measurements of a 130nm CMOS chip show that this combination gives a stability of 5ppm/°C from 20°C to 40°C (14ppm/°C from 20°C to 70°C) at 150nW if temperature changes by 1°C or less every second. The proposed circuit exhibits similar stability to an XTAL with ~7X less power and no off-chip components, provides a low cost ULP solution for wireless sensors and BSNs.

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