Serial Sub-threshold Circuits for Ultra-Low-Power Systems

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Outline

• **Ultra Low Power (ULP) Systems and Sub-threshold**

• **ULP Sub-\(V_T\) Systems: Rethink the Topology**

• **Serial vs Parallel Systems @ Equal VDD**

• **Serial vs Parallel Systems @ Equal Speed**

• **Serial Components in Parallel Systems**
Ultra Low Power Systems

- RFID tags
- Wireless Micro-sensors
- Implantable, Wearable Medical Devices

Key features:
- Small Form Factor
- Remote, Inaccessible Locations

Thus, must have Long Battery Life

=> Low E consumption
ULP Systems: DESIGN FOR SLEEP

• Long Sleep Times:
  ▪ 0.25 sec: Heart Rate
  ▪ 1 Minute: Blood Pressure
  ▪ 1 Hour: Temperature
  ▪ 1 Day: Structural Health

• Total E = Active E + Sleep E

• DESIGN FOR SLEEP MODE: Focus on Reducing Leakage
Active and Sleep Modes

**ACTIVE MODE Energy Components:**

- Dynamic Energy = $C \cdot V^2$
- Leakage Energy = $V \cdot I_{lkg\_active} \cdot \text{Delay}$
- $I_{lkg\_active}$ -> Active Mode Leakage

**SLEEP MODE Energy Components:**

- Sleep Mode Leakage Energy
  
  $= V \cdot I_{lkg\_sleep} \cdot \text{Sleep\_Time}$

- $I_{lkg\_sleep}$ -> Sleep Mode Leakage
Lower VDD => Lower Energy, Leakage: Sub-$V_T$

- Lowering VDD, Lowers:
  - Dynamic Energy $\sim V^2$
  - Leakage Current $\sim \exp(V)$

Strong-Inversion Design:
- High Active E & Leakage

Leakage Reduction:
- Power Gating
- Rev Body Bias
ULP systems put a much tighter constraint on leakage…. Much more so than Conventional Digital Systems

While going into \( \text{Sub-}V_T \),

Should the topology remain the same?
ULP Systems need a Small, Less Leaky Topology

WHY:
DESIGN FOR SLEEP!

TRADEOFF:
Slower Operation

How can this be overcome?
Making the Small, Slow Topology Faster

But why more E-efficient even after the VDD increase?
Sub-$V_T$: Helps Increase Speed @ Very Little Energy-Cost

Note: Normalized Data
Sub-$V_T$: Helps Increase Speed @ Very Little Energy-Cost

Note: Normalized Data
Making the Small, Slow Topology Faster

How do we make the Logic System Smaller & Less Leaky?
Small, Less Leaky Systems: By Lowering System Level Bit Width

• What is System Level Bit Width?
  – Number of bits processed concurrently
  – System Bit Width = 1 => Fully Serial System

• Smaller Bit Width means:
  – Less number of leakage paths
  – But... More cycles needed to finish the same operation

Varying System Bit Widths:
Intel 8 bit and ARM 32 bit processors
Why Lesser Leakage?

4b Ripple Carry Adder:

Serial Adder:
- Needs 4 cycles
- Lesser $I_{lkg}$
Lowering System Level Bit-Width

Systems compared:

- 1b SA-1
- 16b KSA-16
- 32b KSA-32

SA : Serial Adder

KSA: Kogge-Stone Adder
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Leakage and Delay @ Equal VDD

VDD = 300mV, data using 22nm PTM

Serial Systems Help Lower $I_{lk}$
Active E @ Equal VDD

Serial Systems help LOWER Active E:

- Almost no glitching
- Super-linear Area saving

VDD = 300mV, data using 22nm PTM
Total E @ Equal VDD

Higher the sleep time, higher the benefit of a Serial System

We take $I_{\text{lkg\_sleep}} = 0.1 \times I_{\text{lkg\_active}}$
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## Active & Total E @ Equal Speed

<table>
<thead>
<tr>
<th>Sleep Time</th>
<th>Total E Consumed (pJ)</th>
<th>1b SA-1</th>
<th>16b KSA-16</th>
<th>32b KSA-32</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zero</td>
<td>0.06</td>
<td>0.10</td>
<td>0.10</td>
<td></td>
</tr>
<tr>
<td>10us</td>
<td>0.21</td>
<td>0.80</td>
<td>0.96</td>
<td></td>
</tr>
<tr>
<td>1ms</td>
<td>14.90</td>
<td>70.50</td>
<td>85.90</td>
<td></td>
</tr>
<tr>
<td>VDD used</td>
<td>350mV</td>
<td>250mV</td>
<td>200mV</td>
<td></td>
</tr>
</tbody>
</table>

Even at the higher VDD a Serial System has lower:
- Active E
- Sleep E

**Note:** Delay kept at 0.1us
Conclusions @ Equal Delay

✓ In Sub-$V_T$, at slightly higher VDD, a Serial System becomes as fast as a Parallel System

✓ Even at the higher VDD, a Serial System has lower Active E & Sleep E

The constraint is that the ENTIRE system must be Serial
Vision of a Fully Serial System

• What’s already being done serially?
  – Successive Approximation Register (SAR) ADC
  – Radio / Wireless Communication

• Thus, i/p and o/p are already serial

• Examples of Serial Architectures:
  – Serial DSPs (Distributed Arithmetic, R. Amritharajah, et al, 2005)
  – Serial Architectures used in RFID chips
Serial Components in Parallel Systems

P-S and S-P interfaces will have:

- Active E overhead
- But we still get Leakage Current benefit

32b addition system with 32b KSA

32b addition system with a SA
32b system with a Serial Adder block

Parallel System with a Serial Adder Block:

- Has Higher Active E
- **But Helps Save** Sleep E
Contributions

• Small Bit-Width systems help save:
  – Active Mode E & Sleep Mode E
  – Can operate as fast as parallel systems by increasing VDD

• In the sub-$V_T$ regime:
  – Simple topologies are more E efficient
  – Speed can be increased by increasing VDD @ little E cost

• Be flexible to “Re-Think the Topology”
  – As “porting” doesn’t lead to most E-efficient solution
  – Specially when design constraints change significantly
Thank you for your Time!
Backup slides ahead
ULP applications and Sub-$V_T$

- Energy consumed per operation is minimized with VDD in Sub-$V_T$

- As VDD increases:
  - Delay decreases
  - Leakage energy decreases
  - Dynamic energy increases
  - Total energy demonstrates a minima
Energy, Delay eqns above and below $V_T$ are DIFFERENT

In Strong Inversion:
12x Speed-up costs 20x in Energy

In Sub-$V_T$:
12x Speed-up costs ONLY 1.3x in Energy
Results across a VDD range

- Active energy of 1b system < 32b system at all VDD points
- 15x benefit in Active Mode POWER at all VDD points
## Equal Delay vs Equal VDD

### Table: Power Consumption Comparison

<table>
<thead>
<tr>
<th>Topology</th>
<th>Zero Sleep</th>
<th>10µs</th>
<th>1s</th>
<th>$P_{\text{lk}}$</th>
<th>$V_{\text{DD}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1b SA-1</td>
<td>0.06</td>
<td>0.21</td>
<td>14919</td>
<td>0.15</td>
<td>0.35</td>
</tr>
<tr>
<td>16b KSA-16</td>
<td>0.10</td>
<td>0.80</td>
<td>70552</td>
<td>0.70</td>
<td>0.25</td>
</tr>
<tr>
<td>32b KSA-32</td>
<td>0.10</td>
<td>0.96</td>
<td>85852</td>
<td>0.86</td>
<td>0.20</td>
</tr>
</tbody>
</table>

**Notes:**
- All systems working @ 10MHz.
- @ 1 SEC sleep time, 1b system has **5.7x lesser** E than 32b system.

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<tr>
<td>1b SA-1</td>
<td>0.05</td>
<td>0.07</td>
<td>2.72</td>
<td>2723</td>
</tr>
<tr>
<td>16b KSA-16</td>
<td>0.10</td>
<td>0.48</td>
<td>38.10</td>
<td>38096</td>
</tr>
<tr>
<td>32b KSA-32</td>
<td>0.10</td>
<td>0.96</td>
<td>85.85</td>
<td>85852</td>
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**Notes:**
- All systems working @ equal VDD.
- @ 1 SEC sleep time, 1b system has **32x lesser** E than 32b system.

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**Summary:**
- At EQUAL DELAY, 1b systems are STILL MORE E efficient than 32b systems, though the **benefit comes down** from 32x to 5.7x.
Serial Systems become Pareto-optimal in Sub-$V_T$

Below a certain E-D point, 1b system has lesser energy for the same delay

Pareto-optimal E-D curves across sub-threshold and strong-inversion:
(a) active mode energy
(b) total energy with 10µs of sleep time.
Vision of a Fully Serial System

• Data enters 1b per clock cycle

• Every 32 cycles, a word:
  – Streams through the system
  – Undergoes processing
  – Is Communicated off-chip using the wireless link.