Exploring Circuit Robustness to Power Supply Variation in Low-Voltage Latch and Register-Based Digital Systems

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Motivation and Background

Shrinking devices + Higher operating speeds $\rightarrow$ Higher operating currents $\rightarrow$ IR drop + L($dI/dt$)

Motivation and Background

Source: http://www.ansys.com/Products/Electronics/Option-SIwave-PSI-Solver
Motivation and Background

Parasitics (Package, PCB, regulator, chip) ➔ Power Supply Noise


5/22/16
Motivation and Background

- High Frequency: $L \frac{di}{dt}$, package resonance

- Low Frequency: Voltage Regulator, IR drop

Source: http://electronicdesign.com/boards/understanding-power-integrity-system-wide-challenge

Source: http://www.soccentral.com/results.asp?EntryID=19453
Outline

- Problem Statement
- Overview of prior work
- Proposed solution and hypothesis
  - Evaluation of latch-based pipelines in presence of power supply noise
  - All-digital ULP power supply droop measurement
- Measured Results
- Summary and Conclusion
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Problem Statement

Metastability ➔ Timing errors ➔ Performance degradation and yield

\[ T_{\text{clk\_period\_reg}} > T_{\text{ck-q}} + T_{\text{prop\_delay}} + T_{\text{setup}} - T_{\text{clock\_skew}} \]

\[ T_{\text{prop\_delay}} > T_{\text{hold}} + T_{\text{clock\_skew}} \]
Problem Statement

- Self-Powered systems are severely energy-constrained
- Small form-factors
- Longer operational lifetime for ubiquitous deployment
- Supply voltage variation (Harvesting conditions, Regulator drift etc.)

=> Need for a compact, ULP supply-voltage monitor and resiliency to voltage variation

Source: http://inertia.ece.virginia.edu/engineering-research/body-area-sensor-networks
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Overview of Prior Work

- Adaptive clock distribution and in-situ timing error detection and correction [1] ➔ Area


- Decoupling capacitors [4] ➔ Gate leakage

=> Need low cost, compact, ULP supply voltage droop monitors in high-efficiency voltage regulators for ULP systems
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Proposed Solution and Hypothesis

- Power supply noise in latch-based vs. register-based implementations
  - Time borrowing and transparency window in latches can help in resolving metastability issues
  - Higher operating speeds in latches can reduce leakage energy in low VDD operation
- Propose an all-digital ULP droop measurement scheme with current-starved ROs and digital logic for calibration
Block Diagram
Block Diagram

- Noise-Source
- Latch-based FIR
- Register-Based FIR
- Shared Scan-In
- Shared Scan-Out
- VDD_LAT
- CK1
- CK2
- VDD_DROOP
- Ring Oscillator
- Counter
- Scan-Out for Droop Meas
- Counter and Comparator
- Enable/Disable
- VDD_CLEAN
- Clock Source
- VDD_NOISE
- VDD_REG
- CK
- VDD_CLEAN
- Ring Oscillator
- Enable
- LFSR
Latch-based implementation

- Extra timing window in latch-based pipeline to resolve metastability
- Hold margins can be improved using non-overlapping clocks for launch and capture
- Higher operating speeds can amortize higher leakage energy in sub-$V_T$
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Latch-based vs. Register-based implementation: Test setup

- 16-bit, 32-tap FIR filter used as DUT. Implemented using both latches and flip-flops.

- Latch-based implementation utilizes non-overlapping clocks (CK1 and CK2) for launch and capture → Improved hold-margins
Latch-based FIR implementation - Measured Waveforms

 clk | X  0 000
 clk1 | X  0 001
 clk2 | X  0 000
 scan_clk | X  0 000
 en_1 | X  0 011
 out_sel | X  0 011
 rst | X  0 011
 scan_en_in | X  0 000
 scan_en_out | X  0 011
 scan_in | X  0 000
 scan_out | 1  0 001

1MHz System Clock
1.43MHz Dual Phase Non-Overlapping Clocks
1MHz Scan Chain Clock

Enable Latch FIR Block
De-Assert Reset
Assert Scan enable
Configuration and Data
Trigger
Output
Latch-based vs. Register-based implementation - Measured Results

- **25-37% Improvement in energy-efficiency at low VDDs (< 0.6V)** in latch-based implementation in presence of low-frequency supply noise

- **44-120mV external 1kHz supply noise** injected for testing
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All-Digital on-die Power Supply Droop Measurement

- Current-controlled ring oscillator operating at noisy supply
- A counter running at noise-free supply counts RO clock cycles
Droop Measurement Unit: Test setup

On-Chip Noise Injection Circuit

- On-chip noise injection: 8-bit LFSR clocked by a 13-stage current-starved RO couples an 8-bit pseudo-random noise sequence using on-chip capacitor-bank

- Off-chip noise injection: Variable amplitude 1kHz sawtooth waveform coupled to the supply using Agilent 33250A function generator

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All-Digital Power Supply Droop Measurement Unit-Measured Results

### Table

<table>
<thead>
<tr>
<th>VDD (V)</th>
<th>Peak-Peak Droop (mV)</th>
<th>Hex equivalent</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>48</td>
<td>0x07</td>
</tr>
<tr>
<td>0.8</td>
<td>72</td>
<td>0x19</td>
</tr>
<tr>
<td>0.8</td>
<td>104</td>
<td>0x4A</td>
</tr>
<tr>
<td>0.8</td>
<td>128</td>
<td>0x6E</td>
</tr>
</tbody>
</table>

Proxy for Supply droop magnitude

### Graph

- **Supply Voltage (V)**
- **Power (µW)**
- **Change in frequency with droop**
- **VDD with droop**
- **50µs**

- 170mV p-p droop

- **0.9µW at 0.75V**
### Droop Measurement Unit-
Comparison with prior work

<table>
<thead>
<tr>
<th></th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>16nm FinFET</td>
<td>90nm bulk</td>
<td>0.13µm bulk</td>
<td>0.13µm bulk</td>
</tr>
<tr>
<td><strong>Supply Voltage</strong></td>
<td>0.7-0.95V</td>
<td>0.7V-1.3V</td>
<td>0.74-1.3V</td>
<td>0.5-0.8V</td>
</tr>
<tr>
<td><strong>Analog/Digital</strong></td>
<td>Digital</td>
<td>Analog</td>
<td>Digital</td>
<td>Digital</td>
</tr>
<tr>
<td><strong>Area</strong></td>
<td>2590µm²</td>
<td>–</td>
<td>9060µm²</td>
<td>7100µm²</td>
</tr>
<tr>
<td><strong>Power Consumption</strong></td>
<td>2.5mW at 0.9V</td>
<td>–</td>
<td>46.4-56µW at 0.81V</td>
<td>0.9µW at 0.75V</td>
</tr>
<tr>
<td><strong>Max Droop Range</strong></td>
<td>90mV at 0.9V</td>
<td>270mV at 1V</td>
<td>189mV at 0.81V</td>
<td>44-170mV at 0.5-0.8V</td>
</tr>
<tr>
<td><strong>High/Low frequency</strong></td>
<td>High</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
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Summary

- We evaluated the impacts of power supply noise in a latch-based implementation of an FIR filter and compared with a register-based implementation

  - Time borrowing and transparency windows in latch-based pipelines help in resolving metastability issues
  
  - Higher operating speeds in a latch-based pipeline amortized leakage energy in low VDD operation

- We presented an all-digital ULP droop measurement scheme for ULP systems
References


Thank You!