Exploring Circuit Robustness to Power Supply Variation in Low-Voltage Latch and Register-Based Digital Systems

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***Abstract*—This paper compares the impact of power supply variation on the performance of register-based and latch-based digital circuits. A 32-tap, 16-bit FIR filter is fabricated using both flip-flops and latches in a 130nm CMOS process. Measurements show 25-37% improvement in energy-efficiency for the latch-based implementation operating below 0.6V subject to 44-120mV, 1 kHz peak-peak V_{DD} ripple. This paper also presents a low-power, low-frequency droop measurement technique using digital circuits, which consumes 0.9µW at 0.75V.**

Keywords—power supply noise; droop; voltage regulation; latch-based circuits; variation tolerance

I. INTRODUCTION

Variation in on-chip power supply continues to be a major challenge in modern CMOS processes due to technology scaling resulting in increasing device densities and operating currents. Since the lengths of global wires such as power and ground lines do not scale at the same rate as device dimensions, IR-drop continues to increase in deep-sub-micron processes. Since most modern microprocessors operate at clock frequencies in the GHz regime [1], such systems are most susceptible to power supply overshoots and undershoots (ΔV) given by:

$$\Delta V = IR + L\frac{\Delta I}{\Delta T}$$

While supply overshoots can cause reliability issues such as gate-oxide breakdown and hot-carrier injection (HCI), supply undershoots can result in timing violations such as setup-time and hold-time failures. Thus power supply droops can limit the maximum operating frequency (F_{MAX}) of a modern microprocessor. Variation in the power supply can result in timing errors in low-voltage circuits as well [8]. This paper addresses power supply droop detection using digital circuit techniques and compares resilience to power supply variation at lower supply voltages using latch-based and register-based implementation schemes.

An *LΔI/ΔT* event occurs if there is a sudden change in the current consumption, especially when the microprocessor switches from one operating mode to another, resulting in high-frequency overshoot or undershoot noise. Resonant supply noise in the mid-frequency range is another source of power supply noise, which results mainly from resonance of the package inductance and the decoupling capacitors [5]. During dynamic voltage scaling (DVS), the slow transient response time of voltage regulators can result in low frequency droops. Fig. 1 describes the two major sources of power supply fluctuations. High-frequency noise is generally induced on the supply due to *LΔI/ΔT* events and impacts timing in local circuit paths. Noise due to package resonance and low-frequency droops takes time to recover and thus is present for multiple clock cycles and impacts performance globally across the chip.

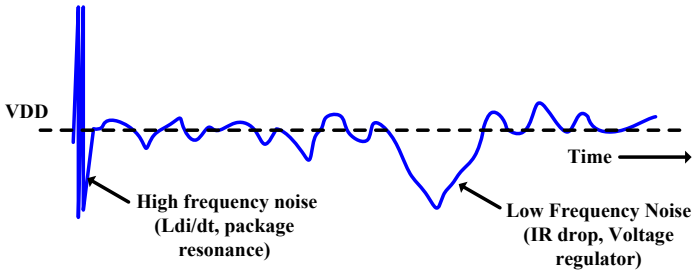

Fig 1: Examples of power supply noise [4]

Existing work in literature such as [2] has proposed on-die dynamic voltage monitoring and adaptive clock distribution schemes to enable tolerance to power supply variations across a wide operating range. In [3], techniques for timing error detection and correction are proposed to reduce metastability occurring due to dynamic power supply and temperature variations. Analog techniques have been employed in [4] where on-die sensors are distributed to monitor peak overshoots and undershoots. Dynamic IR-drop can be reduced by adding decoupling capacitors. Noise on the power supply in the low to mid-frequency range can be compensated by using active decoupling capacitors [5]. However adding decoupling capacitors increases gate leakage. Analog droop monitors [4] and metastability detectors [3] consume higher quiescent currents. Hence such techniques cannot be applied directly in subthreshold processors such as [6][9] which are used in energy-constrained systems such as wireless sensor nodes and other applications related to the IoT.

In this paper, we analyze the impact of low-frequency power supply droops on both register-based and latch-based

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implementations of a 32-tap Finite Impulse Response (FIR) filter across a wide range of supply voltages. FIR filters play an important role in most low-power as well as high-performance DSP applications [11]. We investigate the circuit robustness to power supply variation for both latch-based and register-based versions of the FIR filter by measuring the energy-delay (ED) trends. We use ED curves as a metric to evaluate the resiliency of a synthesized digital circuit (in this case a FIR filter) to power supply variations. We implement a low-power technique to measure the low-frequency droop present in the power supply and also present a scheme to inject on-die supply noise using a pseudo-random Linear Feedback Shift Register (LFSR) unit. This paper is organized as follows: Section II describes the block diagram, the droop measurement, and droop injection circuits. Section III presents the measurement results. Section IV concludes the paper.

II. ARCHITECTURE

A. Block Diagram

Fig 2 describes the block diagram of the system designed for analyzing and comparing the impact of power-supply variation on latch-based and register-based versions of the FIR filter.

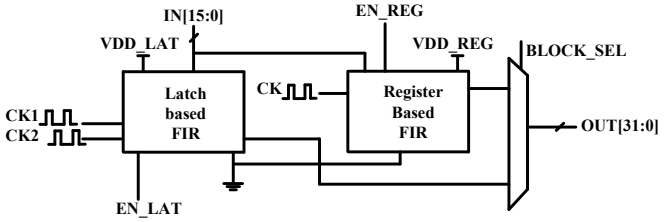

Fig 2: Block Diagram for the CMOS test chip

We implement a 16-bit, 32-tap FIR filter using both flip-flops and latches. For the latch-based implementation, we incorporate a dual-phase non-overlapping clock architecture to reduce the probability of hold-time failures. Both the latch-based and register-based FIR filters have dedicated enable signals and supply rails while they share a common reset and ground rail. A global block-select signal helps in selecting the 32-bit output from each FIR filter.

B. Proposed Droop Measurement Technique

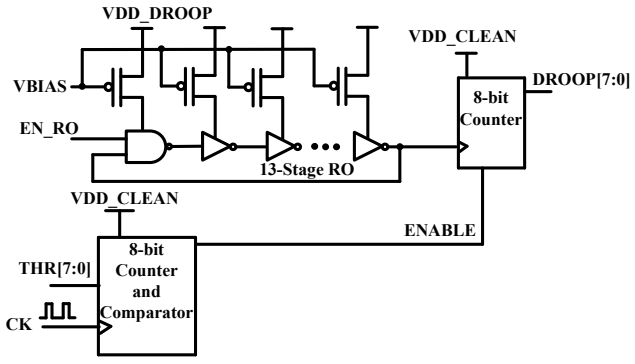

Fig 3: Droop measurement circuit

Fig. 3 describes the on-chip droop measurement scheme. The core of the droop measurement circuit is an on-chip 13-stage current-starved ring oscillator (RO) operating from the supply rail, VDD_DROOP which contains voltage droops. The ring oscillator is biased in subthreshold by an external bias signal, VBIAS, which can be generated by an ultra-low-power bandgap reference such as [7]. An 8-bit digital counter and comparator is powered by a clean, well-regulated supply without ripple, VDD_CLEAN. This 8-bit counter and comparator logic compares the number of clock cycles with a programmable 8-bit user-defined threshold, THR and generates an enable/disable signal to count the number of RO clock cycles denoted by DROOP. The number of RO clock cycles will vary depending on the magnitude of droop present. The difference between DROOP and THR provides an 8-bit digital proxy measurement for the amount of supply droop present. At a system-level, VDD_CLEAN can be obtained from a voltage regulator such as the buck-boost regulator proposed in [6]. An on-chip voltage regulator needs to provide high conversion efficiency for a target load current range. For a fixed conversion efficiency of a regulator, a lower-power droop monitoring circuit would reduce the overhead on the limited power budget of an energy-constrained system.

C. Proposed Droop Injection Scheme

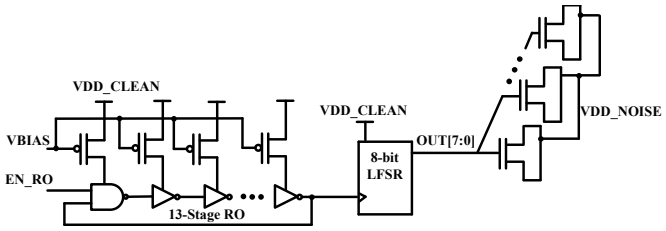

Fig 4: Droop injection circuit

Fig. 4 describes the droop injection circuit used to inject supply noise onto the supply rails for test purposes. A 13-stage current starved RO operating from a clean supply voltage devoid of supply noise, VDD_CLEAN provides the clock to an 8-bit LFSR unit to generate an 8-bit pseudo-random sequence. This 8-bit sequence couples pseudo-random noise onto the supply rail, VDD_NOISE using MOS capacitors. The RO clock period can be controlled externally using the bias signal, VBIAS, to provide the desired clock frequency. The injected droop can be measured by the droop measurement scheme described in Fig. 3

D. Synthesis and Timing Constraints

A latch-based pipeline stage typically allows the designer to achieve higher performance than a register-based implementation owing to time-borrowing and allowing greater setup-time margin as compared to a flip-flop. Assuming no clock skew, the setup-time constraint for a latch is:

$$T_{clk\_period\_latch} + T_{wind} > T_{d-q} + T_{prop\_delay} + T_{setup\_time}$$

where, T_{wind} = transparency window of a latch

$T_{clk\_period\_latch}$ = clock period of latch-based stage

T_{d-q} = input data to latch output delay

T_{prop_delay} = propagation delay

T_{setup_time} = setup time constraint

Similarly for a flip-flop based design,

$$T_{clk\_period\_FF} > T_{clk-q} + T_{prop\_delay} + T_{setup\_time}$$

where, $T_{clk\_period\_FF}$ = clock period of a flip-flop based stage

T_{clk-q} = clock to flip-flop output delay

Hence, $T_{clk\_period\_latch} < T_{clk\_period\_FF}$ which means that a latch-based pipeline stage can operate at a higher clock frequency than a flip-flop based stage. Moreover, since a latch-based pipeline provides an additional transparency window, the incoming data has an additional setup-time margin equivalent to T_{wind}, which aids in resolving metastability issues arising due to power supply variations and low-frequency supply noise. Short-paths in a latch-based design can be avoided as long as,

$$T_{wind} + T_{hold\_time} < T_{d-q} + T_{prop\_delay}$$

where, T_{hold_time} = hold time constraint

Although a flip-flop based timing path has greater hold-time margin as compared to a latch-based path, this limitation can be offset by employing out-of-phase non-overlapping clock signals.

For the latch insertion in the FIR filter, we mapped a 16-bit, 32-tap FIR filter to logic gates using commercial synthesis tools. To control time-borrowing and allowing latch insertion only when necessary, custom scripts were used to replace each register with a pair of master and slave latches clocked by out-of-phase non overlapping clocks [10]. After inserting latches, timing optimization and logic restructuring was performed to balance all pipeline stages to achieve timing closure at 200kHz and 0.5V.

III. MEASUREMENT RESULTS

Fabricated in a 130nm CMOS process, the testchip was packaged in a 64-pin PGA package for testing convenience. A Link Instruments IO3200 pattern generator/logic analyzer module was used to provide input patterns and off-chip clock signals to both latch-based and register-based FIR filters. Current measurements were performed using a Keithley 2401 sourcemeter. External droop was added to the supply with a function generator. A 1 kHz saw-tooth waveform of varying peak-to-peak amplitude was coupled to the power supply.

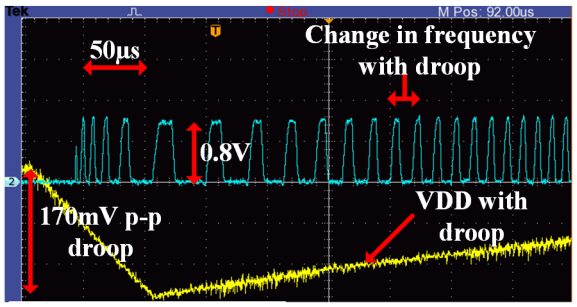

Fig 5: Variation in RO frequency with supply voltage

TABLE I. MEASURED HEX EQUIVALENT OF DROOP (THR: 0xAA)

VDD (V)	Peak-Peak Droop (mV)	Hex equivalent
0.8	48	0x07
0.8	72	0x19
0.8	104	0x4A
0.8	128	0x6E

External noise and supply droop can be injected off-chip by coupling a fast rising ramp signal to the power supply using a large coupling capacitor in the order of 47µF or higher. Fig. 5 shows the oscilloscope waveform of a power supply where external noise has been added. The variation in frequency of the RO described in Fig. 3, which operates at VDD_DROOP, is shown. Table I shows the measured hex-equivalent of the droop present on a 0.8V supply with THR set at 0xAA. Fig 6 shows the variation of power consumption of the droop measurement unit with the supply voltage. The measured power includes power consumption of the ring oscillator, counters and comparator logic. Measurements show that the droop measurement circuit consumes less than 1.5µW across a range of supply voltage ranging from 0.5-0.8V and can be leveraged in ULP systems such as wireless sensor nodes.

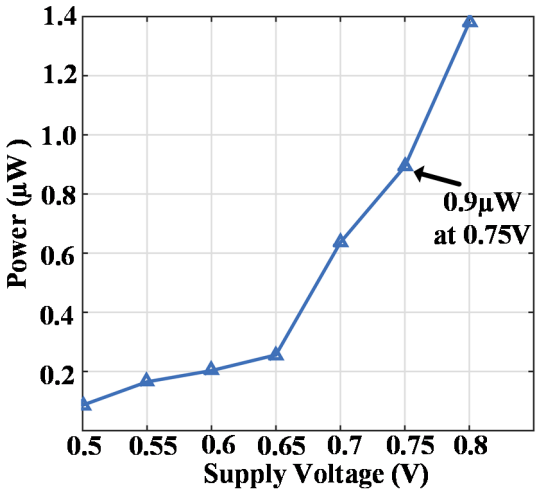

Fig 6: Measured power of droop measurement unit

Fig. 7 shows the energy-delay trends of both the latch-based and register-based FIR filters both with and without externally injected power supply noise (PSN).

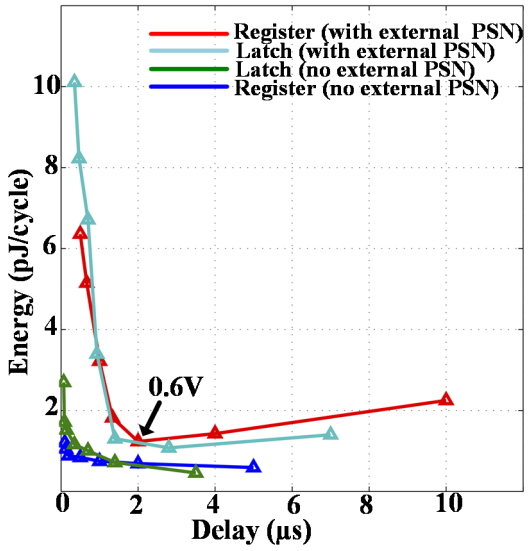

Fig 7: Measured Energy-Delay trends of latch-based and flip-flop based FIR filters

Fig. 7 shows that the latch-based implementation provides 25-37% improvements in energy-efficiency below 0.6V in the presence of 1kHz power supply droop ranging from 44-

120mV. At higher voltages and operating frequencies, the register-based implementation provides better energy-efficiency. This is because active-energy dominates at higher voltages and the latch-based implementation has a higher switching capacitance owing to a dual-phase clocking scheme. Fig. 8 shows a chip micrograph of the implementation.

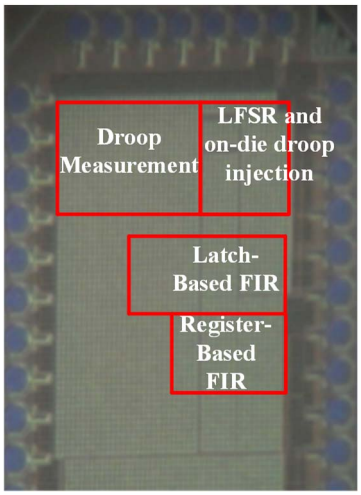

Fig 8: Chip Micrograph

TABLE II. COMPARISON OF DROOP MEASUREMENT UNIT WITH PRIOR WORK

	[2]	[4]	[8]	**This Work**
Technology	16nm FinFET	90nm bulk	0.13µm bulk	**0.13µm bulk**
Supply Voltage	0.7-0.95V	0.7V-1.3V	0.74-1.3V	**0.5-0.8V**
Analog/Digital	Digital	Analog	Digital	**Digital**
Area	2590µm2	–	9060µm2	**7100µm2**
Power Consumption	2.5mW at 0.9V	–	46.4-56µW at 0.81V	**0.9µW at 0.75V**
Max Droop Range	90mV at 0.9V	270mV at 1V	189mV at 0.81V	**44-170mV at 0.5-0.8V**
High//Low frequency	High	High	Low	**Low**

Table II compares the proposed droop measurement scheme with the existing droop measurement techniques in literature. In [2], a dynamic variation monitor (DVM) is proposed to monitor high-frequency voltage fluctuations and consists of and an adaptive clock distribution (ACD) scheme to tune the system clock frequency. The DVM and ACD consume 2.5mW (1% of the total power consumption). In [4], an on-die high-frequency supply droop detector using analog circuit techniques is proposed for noise detection and digital circuits are used for measurement and calibration. In [8], an adaptive clocking scheme using a critical path replica is proposed to modulate the global system clock and local clocks in presence of power supply noise. The droop monitoring circuits in both [2] and [8] monitor supply variation above 0.7V and consume higher power as compared to the proposed droop measurement scheme in this paper.

IV. CONCLUSION

This paper compares the impact of power-supply variation on the energy and performance of latch-based and register-based synthesized digital circuits across a wide-operating range. An all-digital, power-efficient droop measurement and noise-injection technique is discussesd. Measurements show that latch-based circuits provide better energy-efficiency and tolerence to supply variations at lower voltages. Hence a latch-based architecture can be employed in subthreshold processors with variable supply for IoT applications.

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