A 55nm Ultra Low Leakage Deeply Depleted Channel (DDC) Technology Optimized for Energy Minimization in Subthreshold SRAM and Logic

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Outline

- Motivation
- Sub-threshold design challenges
- Technology overview
- Results: technology-circuit co-design
- Comparison
Motivation

Wearable Device Shipments by Device Type and Markets: 2015-2020

- Smart Watches
- Smart Glasses
- Smart Clothing
- Fitness Trackers
- Body Sensors
- Wearable Cameras
- Other Wearables
Motivation

Energy Minimization demands sub-threshold operations.

[Ref.] Naveen Verma Trans. on Elec. 2008
Sub-$V_T$ Challenges

- Reduced drive current ($I_{ON}$)
- Device-to-device mismatch due to huge $V_T$ variation
- High Leakage
- Reduced noise margin
Sub-$V_T$ Challenges

![Graph showing normalized $I_{ON}/I_{OFF}$ ratio for NMOS and PMOS transistors across different process corners (TT, FF, FS, SF, SS). The graph demonstrates higher variation and Ion/Ioff reduction.]

[Ref.] Harsh Patel et al., ISQED 2016
Available Solutions

Technologies:

<table>
<thead>
<tr>
<th>[3]</th>
<th>[6]</th>
<th>[7]</th>
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<tbody>
<tr>
<td>32nm HK-MG</td>
<td>22nm ETSOI</td>
<td>FinFET</td>
</tr>
<tr>
<td>Provides higher $I_{ON}$; Reduced $I_{OFF}$</td>
<td>Improves performance</td>
<td>Improves performance</td>
</tr>
<tr>
<td>$V_{DD}$ Scaling is limited to 1.0V (No sub-$V_{TH}$ operation)</td>
<td>Doesn’t address $V_{TH}$ variation (No stable operation)</td>
<td>Still higher $V_{TH}$ variation (No stable operation)</td>
</tr>
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Available Solutions
Circuit Design:

<table>
<thead>
<tr>
<th>High-$V_T$</th>
<th>Thick-Ox</th>
<th>Body Biasing</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>channel impurities [9]</strong></td>
<td><strong>Gate die-electric</strong></td>
<td><strong>Control body of FETs</strong></td>
</tr>
<tr>
<td>- sub-threshold leakage ($I_{OFF}$)</td>
<td>- Gate-leakage</td>
<td>- sub-threshold leakage ($I_{OFF}$)</td>
</tr>
<tr>
<td>- RDF</td>
<td>- $V_T$ Variation</td>
<td>- Junctional leakage</td>
</tr>
<tr>
<td>- Junctional leakage</td>
<td>- Device mismatch</td>
<td>- Saturates with increase in degree</td>
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Technology Overview

Technology:
Deeply Depleted Channel (DDC)

Gate Length (nm):
55

Devices:
Ultra-Low Leakage (ULL)

Enabling Circuit-level Technique:
Reverse Body Biasing (RBB)
Sub-\(V_T\) Challenges: Reduced \(I_{ON}\)

Sub-threshold Optimization:
- DDC shows higher \(I_{ON}/\mu m\)

Measured \(I_D\) vs \(V_{GS}\) across multiple samples and across process corners
Sub-$V_T$ Challenges: $V_T$ variation

$V_T$ variation spread comparison

~30% $V_T$ variation reduction
Sub-$V_T$ Challenges: $V_T$ variation

- DDC ULL
- Non-DDC Standard-$V_T$
- Non-DDC Low-$V_T$

Less Variation:
- 67% compared to SVT
- 45% compared to LVT

$V_T$ roll-off comparison
Sub-$V_T$ Challenges: Leakage

75X leakage reduction with higher degree of RBB

75X 6T bitcell leakage minimization with a higher degree of RBB.
Sub-$V_T$ Challenges: Noise Margin

Butterfly curves for SRAM 6T bitcell: DDC ULL vs. non-DDC (conventional) bitcell
Test-Chip Results

- Circuit techniques (sub-$V_T$ operation and RBB) are co-designed with the technology to maximize the energy power saving.

- 1Kb 6T SRAM, 32-bit FIR, and Ring. Osc.

Fabricated chip with 1kb SRAM and 16-bit FIR block
Test-Chip Results: SRAM

6X Energy reduction using RBB

Effectiveness of RBB: Higher leakage reduction and lower $I_{ON}$ reduction
Test-Chip Results: FIR

Energy minimization using RBB (by leakage reduction)

Energy (pJ/cycle)

Delay (μs)
Test-Chip Results: RO

RBB is more effective at lower $V_{DD}$s (Sub-$V_T$ range)
## Comparison

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<thead>
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<th>This work</th>
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<th>[17]</th>
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</thead>
<tbody>
<tr>
<td>Tech. (nm)</td>
<td>55</td>
<td>65</td>
<td>65</td>
<td>65</td>
<td>65</td>
</tr>
<tr>
<td>Cell Type</td>
<td>6T</td>
<td>8T</td>
<td>9T</td>
<td>14T</td>
<td>8T</td>
</tr>
<tr>
<td>Transistor Type</td>
<td>ULL</td>
<td>NA</td>
<td>Mixed $V_T$</td>
<td>High-$V_T$</td>
<td>Low-Power</td>
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<tr>
<td>Array $V_{MIN}$</td>
<td>0.2V</td>
<td>0.35V</td>
<td>0.3V</td>
<td>0.5V</td>
<td>0.4V</td>
</tr>
<tr>
<td>Energy (fJ/bit)</td>
<td>31.25</td>
<td>870</td>
<td>18.2</td>
<td>14</td>
<td>78</td>
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</table>
References

Thank you!
Sub-V$_T$ Challenges: Increased $I_{\text{Gate}}$

Sub-threshold Optimization:

- Reduced gate leakage (by increasing TOX)
- without impacting $V_T$ variation

Impact of increase in Gate-Oxide thickness (TOX) on $V_T$ variation