Sub-threshold Sense Amplifier (SA) Compensation Using Auto-zeroing Circuitry

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SA Offset voltage

• Voltage offset in SRAM sense amplifiers due to variability causes increased power consumption and degraded performance.

• The effect is more dominant in the sub-threshold region due to the high offset voltage sensitivity to supply voltage and temperature variations.

• Several attempts have been made before to tackle the problem including:
  • Redundancy
  • Transistor upsizing
  • Digitally controlled compensation
Digital Auto-zeroing (DAZ)

• We propose a digital auto-zeroing (DAZ) scheme inspired by analog amplifier offset correction.

• **The main advantages of the approach are**
  • Near-zero offset after cancellation.
  • Automatic temperature, voltage, and aging tracking achievable using a repeated offset calibration phase.
Outline

- **DAZ Circuit**
- Temperature, Voltage and Aging Tracking
- Offset Tuning
- Power Consumption
- Offset Sensitivity
- Chip Measurements
DAZ Circuit

- DAZ circuit applied to a latch-based sense amp with PMOS inputs

- DAZ circuit uses a split-phase clock and charge pump (CP) feedback circuit for repetitive compensation.
DAZ Circuit

- Transistors MC1 and MC2 control the drive strength of the right side of the SA.
- The CP controls the drive current in both MC1 and MC2 to equalize the strength of the SA right and left sides.
Split Phases

• ER1, ENO, ER2, ENI are applied sequentially

ER1: A zero differential input is applied to the sense amp.

ENO: The SA resolves based on its intrinsic offset.

ER2: The differential input is applied to the sense amp.

ENI: The SA resolves based on the differential input.

EN is the SA enable signal
Charge Pump

- The CP circuit charges $C_p$ up or down during ER2 based on the SA intrinsic offset.
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Temperature and Voltage Tracking

• Offset voltage that remains after compensation is simulated for various voltages and temperatures in commercial 45nm process.
Aging Tracking

- The CP boosts Cp voltage to restores the compensated offset voltage after an abrupt increase in MC2 threshold voltage.
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Offset Tuning

- **Settling time:** The difference between the time when the zero differential-input is applied and the time when the voltage of the output capacitor settles.
Offset Tuning

- Accuracy (offset voltage) vs. settling time trade-off through \( C_p \) tuning.

![Settling Time (us) vs. Min Achieved Offset (mv) Graph](image)
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Power Consumption

- The main contribution to the power consumption comes from the continuous calibration.

- Approaches to reduce power consumption
  
  - Minimizing the period of the calibration phase relative to the input phase.
  
  - Shorting the output virtual nodes of the charge pump.
  
  - Avoid toggling the sense amp output during offset compensation phase (ENO).
Short CP virtual nodes

- Shorting the CP output virtual nodes through M11 decreases the leakage by reducing VDS of the switches, leads to smaller settling time.
Avoid continuous toggling of SA output

- Strengthening M9 in the CP circuit relative to M10 avoids the continuous toggling of the SA output.
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Offset Sensitivity

- The sensitivity of the offset compensation depends on:
  - The split phases
  - The charge pump circuit
  - The output capacitance ($C_p$)
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Chip Measurements

• A test chip fabricated in 45nm technology is used to verify the scheme.

• The chip contains one regular SA array for benchmarking and another array that uses the auto-zeroing circuit, with $C_p=0.74\,\text{pF}$.

• Split phase of 1MHz frequency is supplied to the auto-zeroing circuit.
Offset Distribution

- DAZ circuit limited the absolute average value of the offset to 1mV.
Conclusion

• We proposed a circuit that is capable of improving sense-amp offset to near zero, which is valuable for sub-threshold operation due to the heightened effect of mismatch.

• Measurements from a test chip fabricated in 45nm technology showed the circuit ability to improve the offset to 1mV using 1MHz split phase frequency and 0.74pF Cp capacitance.